Application Note: AS8506-AN01 – Standalone Balancer

AS8506

AN01 – Standalone Balancer

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Revision History

Revision	Date	Owner	Description
1.0	26.06.2013	gheh	Initial release
1.1	25.04.2013	gheh	Changed component names

1 General Description

This document describes the AS8506 Standalone Balancer Demo.

This kit demonstrates the AS8506's ability to operate without a microcontroller and firmware. It allows balancing of up to 7 cells autonomously.

The hardware will support li-based cell packs as well as EDLCs.

Number of cells, target voltage as well as over and under voltage can be configured by resistor options.

1.1 Kit Content

The kit consists of one single layer board with an 8 pin battery connector and a push button for activation.

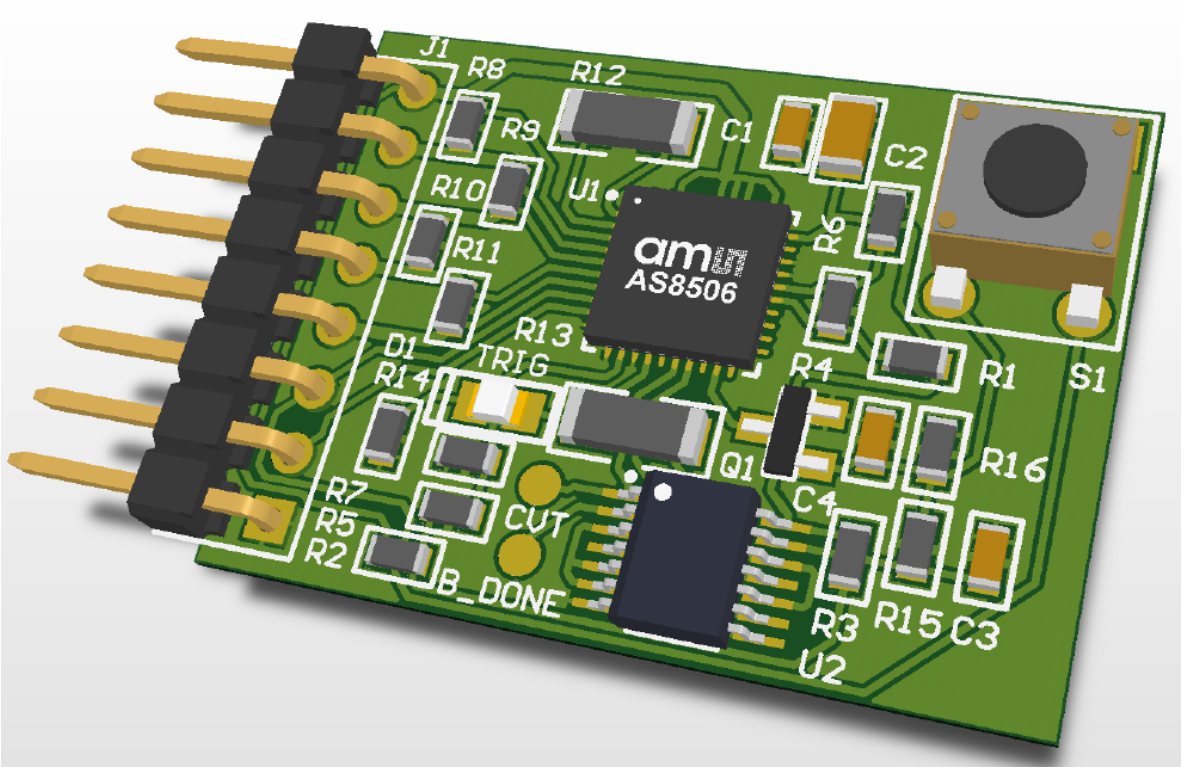

Figure 1: AS8506 Standalone Board

2 Getting Started

To get started configure the device to your cell count and voltage specifications as described in the configuration chapter.

When button S1 is pressed this signal is latched and the balancer first simultaneously compares cell voltages with a reference voltage VREF followed by 7 balancing slots of 1 second each. This

sequence is repeated at a rate of 7 seconds as long as the latch is not reset by the balance done (BD) signal.

Cells which are higher than VREF will sequentially be discharged for 1 second per cell by a charge quanta as defined by the discharge resistor R15 within the 7 second repeating loop until all cell voltages are equal to VREF.

3 Hardware Description

The AS8506 Standalone demo is powered via the battery connected via J1. Unconnected pins (in case lower cell counts then 7 are used) are shorted out by the bridging resistor and can be left unconnected.

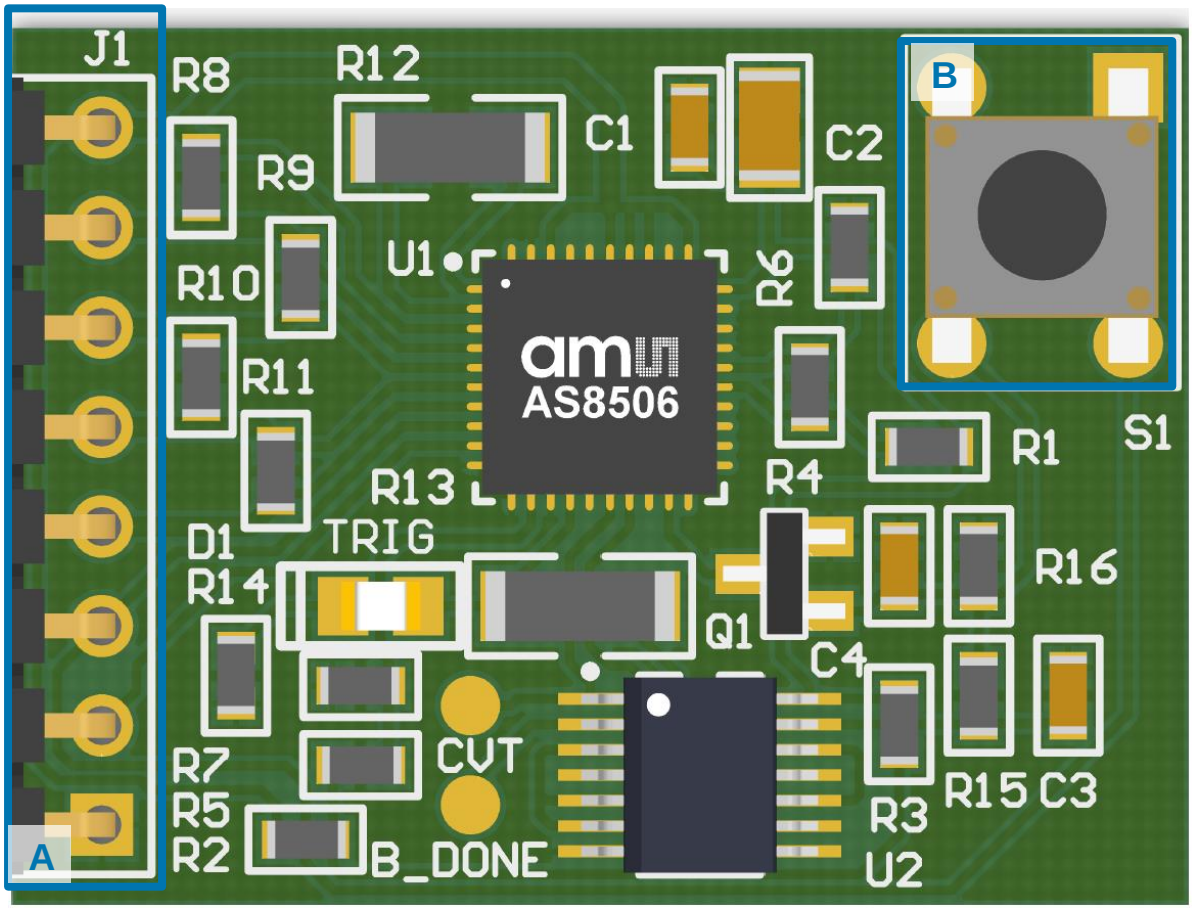

Figure 2: PCB Diagram

Label	Name	Designator	Description	Info
A	BATT	J1	Battery Connector	Connects to 3 to 7 cells GND on the bottom

Label	Name	Designator	Description	Info
B	BUTTON	S1	Balance button	Press to activate balancing

Table 1: Connection Diagram

4 Configuration

4.1 Number of cells

Minimum number of cells to be balanced is 3 or as many to reach a battery voltage of at least 6V (cell chemistry / technology dependent). A maximum of 7 cells can be balanced by this board!

Remove zero ohm resistors according to table:

Cell-Nr	Remove
3	none
4	R11
5	R11, R10
6	R11, R10, R9
7	R11, R10, R9, R8

Table 2: Cell Adjust

4.2 Cell voltage threshold

Select R1, R4 and R6 to adjust maximum and minimum cell voltage thresholds from the 5V VDD on chip regulator (pin V5V) for cell monitoring!

Any cell exceeding maximum threshold or undershoot minimum threshold will issue CVT_NOK diagnosis and will stop the balancing.

Calculate the resistor values according to the formula:

$$R6 = \frac{THL}{I}$$

$$R4 = \frac{THU - THL}{I}$$

$$R1 = \frac{5V - THU}{I}$$

Where I is typically 100µA and THL and THU are the lower and upper threshold voltages.

The table below shows some typical examples:

Chemistry	THU	THL	R1	R4	R6
LiIon (default)	4.2V	3.0V	8K06	12K	30K
LiFe	3.6V	2.8V	14K	8K06	28K
EDLC	2.7V	0V	22K9	12K	15K

Table 3: Threshold adjust

4.3 Configuration of VREF

There are three options of defining VREF:

1. Internal fixed reference:

   For balancing during constant voltage charge phase VREF is derived from regulated 5V VDD. For this case, zero ohm resistor R3 has to be populated (this is the case when you receive the board). VREF needs to be adjusted dependent on cell chemistry according to the formula:

$$R7 = \frac{VREF}{I}$$

$$R5 = \frac{5V - VREF}{I}$$

   Where I is again 100µA.

   The table below shows some typical examples:

Chemistry	VREF	R7	R5
LiIon (default)	4.2V	43K	8K2
LiFe	3.6V		
EDLC	2.7V		

Table 4: VREF absolute adjust

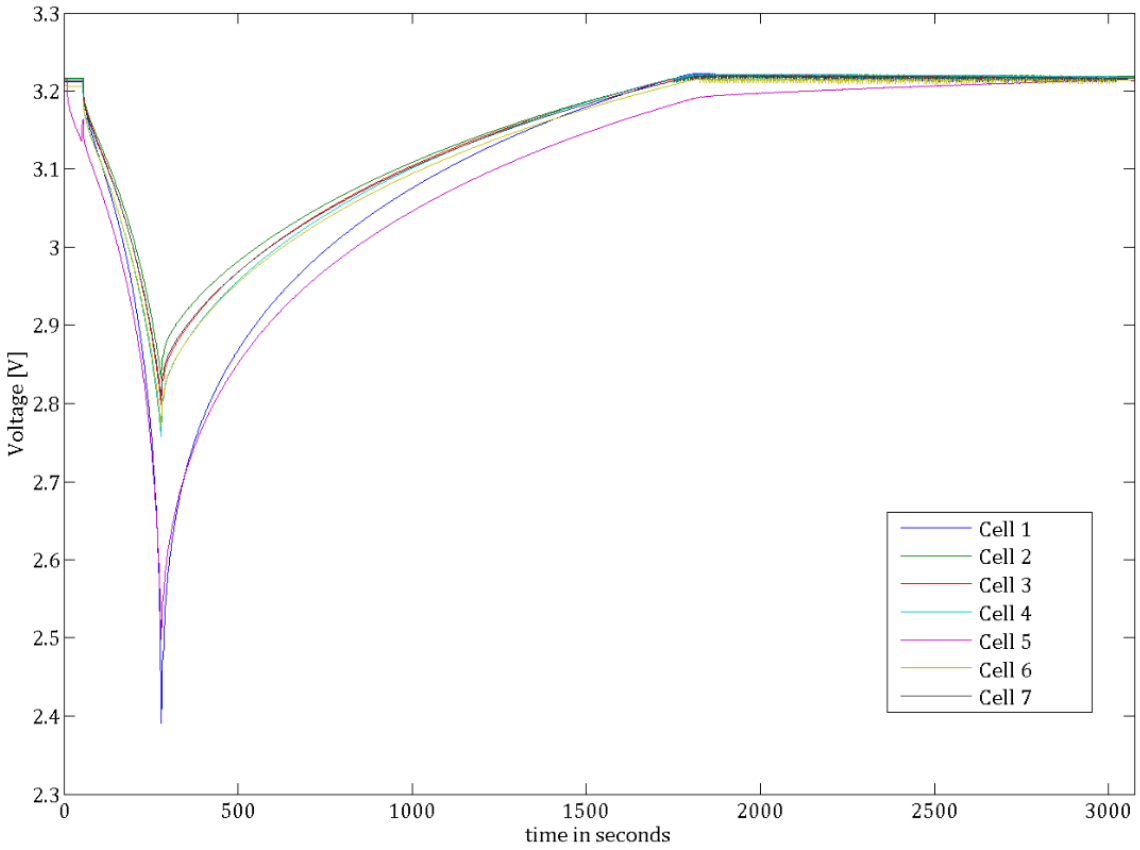

Figure 3: Balancing example during constant voltage charge

In Fig.3 example 7 LFP cells 2,5 Ah are discharged, charged and balanced. Cell number 5 is intentionally further discharged to generate some misbalance. Cell number one has less capacity due to manufacturing spread or accelerated ageing.

2. External fixed reference

   For Balancing towards a fixed reference voltage the VREF can be chosen by an external source in the 1,8V to 4.5V range versus GND. When balancing is triggered and VREF is chosen slightly below lowest cell voltage the demo will equalize all cells towards VREF and stop balancing once all cells are at VREF.

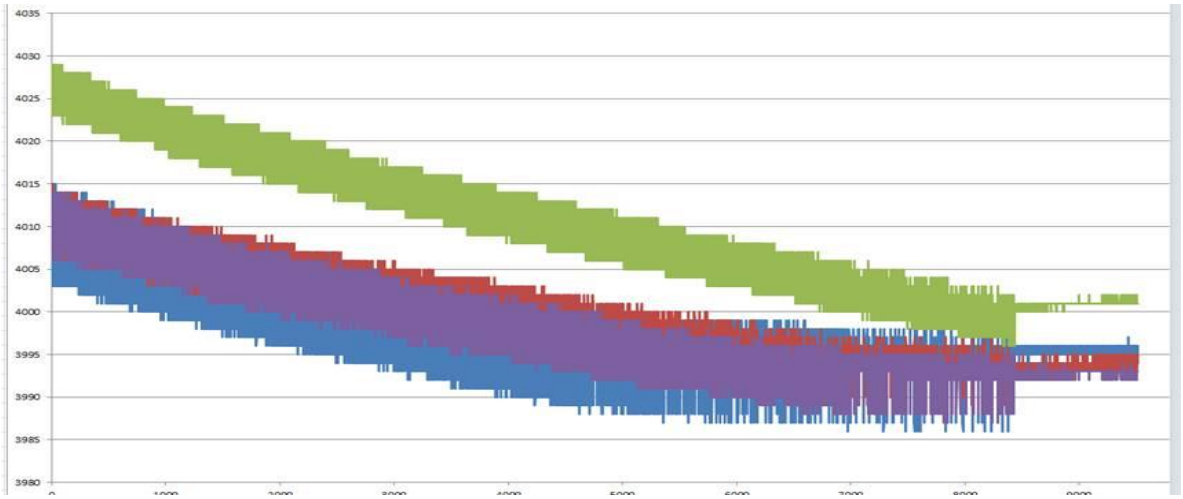

Figure 4: Balancing example towards a fixed reference

3. Close to mean cell voltage

   For balancing close to a mean cell voltage at any SOC level the VREF can be generated by resistive divider from VBAT by placing R2 zero ohm resistor (make sure that R3 is removed). In that case the divider R7, R5 need to be selected according to number of cells according to the following table:

Cell-Nr	R7	R5
3	100K	200K
4	100K	300K
5	30K	120K
6	150K	750K
7	20K	120K

Table 5: VREF relative adjust

Reliable balance done detection might be problematic if the divider ratio does not accurately match the pack size. The divider ratio might need to be set slightly above the actual mean value like 101k in the given example to account for offsets and losses.

5 Board Schematics, Layout and BOM

The AS8506 Standalone demo is a 1-layer FR4 board. It is designed for minimal component count. It's main component is the AS8506 together with a 4001 NAND gate.

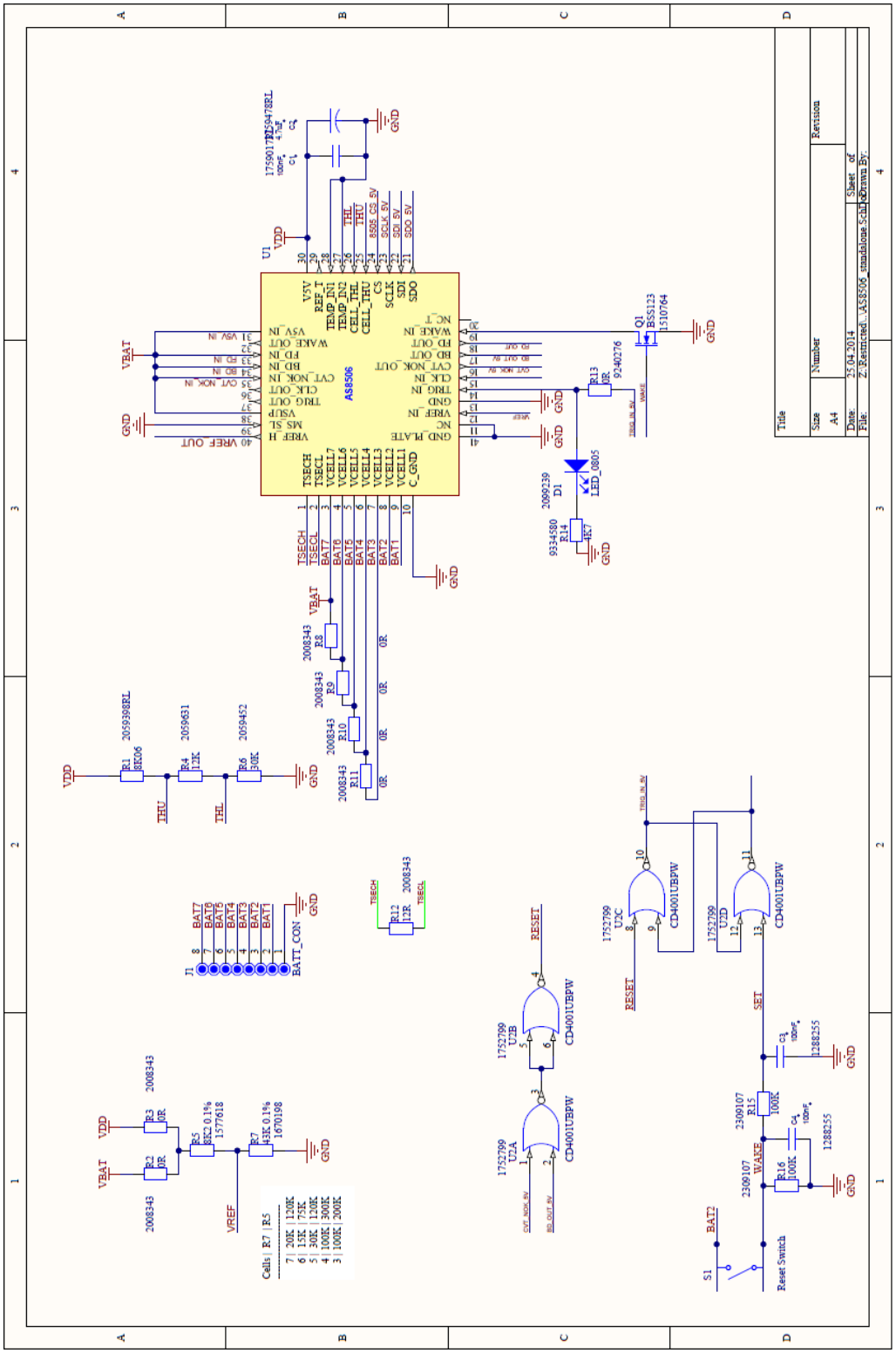

Figure 5: AS8506 Standalone Demo Schematic

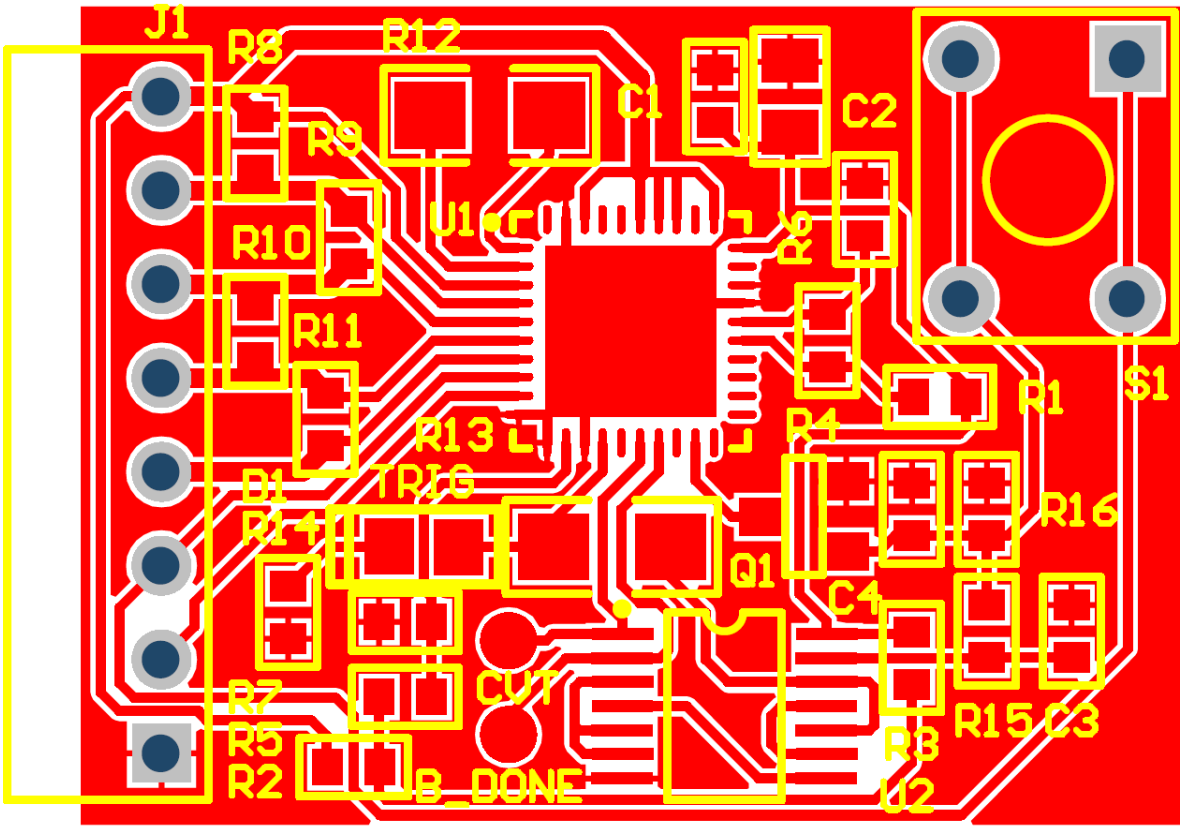

Figure 6: AS8506 Standalone Top

Bill of Materials — AS8506 Standalone Balancer

Company:	ams AG
Originator:	gheh
PCB Name:	AS8506 Standalone Balancer
PCB Version:	0.2
Report Date:	10.09.2013

#	Designator	Comment	Description	Manufacturer	Manufacturer Part Number	Quantity
1	C1	100nF		MULTICOMP	MCCA000160	1
2	C2	4.7uF		MULTICOMP	MCCA000595	1
3	C3	100nF		KEMET	C0603C104K5RACTU	1
4	C4	100nF		KEMET	C0603C104K5RACTU	1
5	D1	LED_0805		KINGBRIGHT	KPT-2012SGC	1
6	J1	BATT_CON				1
7	Q1	BSS123	N-Channel Fet	NXP	BSS123	1
8	R1	8K06		PANASONIC	ERJ3EKF8061V	1
9	R3	0R		BOURNS	CR0603-J/-000ELF	1
10	R4	12K		PANASONIC	ERJ3GEYJ123V	1
11	R5	8K2 0.1%		PANASONIC	ERA3AEB822V	1
12	R6	30K		PANASONIC	ERJ3EKF3012V	1
13	R7	43K 0.1%		PANASONIC	ERA3AEB433V	1
14	R8	0R		BOURNS	CR0603-J/-000ELF	1
15	R9	0R		BOURNS	CR0603-J/-000ELF	1
16	R10	0R		BOURNS	CR0603-J/-000ELF	1
17	R11	0R		BOURNS	CR0603-J/-000ELF	1
18	R12	12R		BOURNS	CR0603-J/-000ELF	1
19	R13	0R		YAGEO (PHYCOMP)	RC1206JR-070RL	1
20	R14	4K7		MULTICOMP	MC 0.1W 0805 5% 4K7	1
21	R15	100K		YAGEO	RC0603FR-13100KL	1
22	R16	100K		YAGEO	RC0603FR-13100KL	1
23	S1	Reset Switch				1
24	U1	AS8506				1
25	U2	CD4001UBPW	Quad 2-Input NOR Buffered B series Gate, 14-Pin SOP, Commerical Grade	TEXAS INSTRUMENTS	CD4001UBPW	1
Approved			Notes			25

Figure 7: AS8506 Standalone BOM

6 Ordering Information

The AS8506 Standalone demo can be ordered via:

Table 11: Ordering Information

Ordering Code	
AS8506-DK-ST	AS8506 Standalone Demo