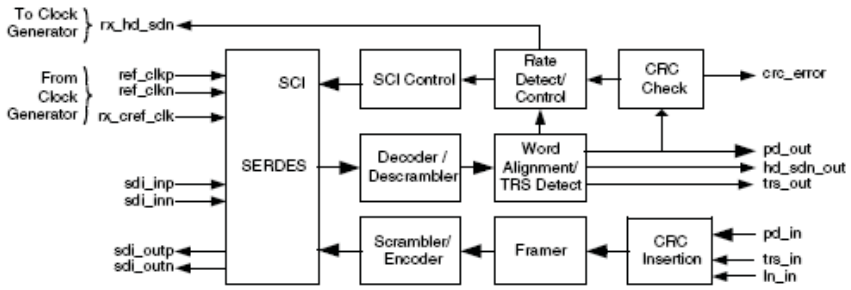
Multi-Rate Serial Digital Interface (SDI) PHY Layer

As the proliferation of HDTV, IPTV and VoD streaming continues, together with the increased functionality and decreasing costs of FPGAs, it is inevitable that these two technologies will converge in the solution space. A key requirement is the ability to transmit, receive, edit, and process uncompressed video. The transceiver portion of this requirement is standardized by the Society of Motion Picture and Television Engineers (SMPTE) through the Serial Digital Interface (SDI) family of standards. These standards define the physical interface and related circuitry needed to transport uncompressed digital video over 75-ohm coax cable.

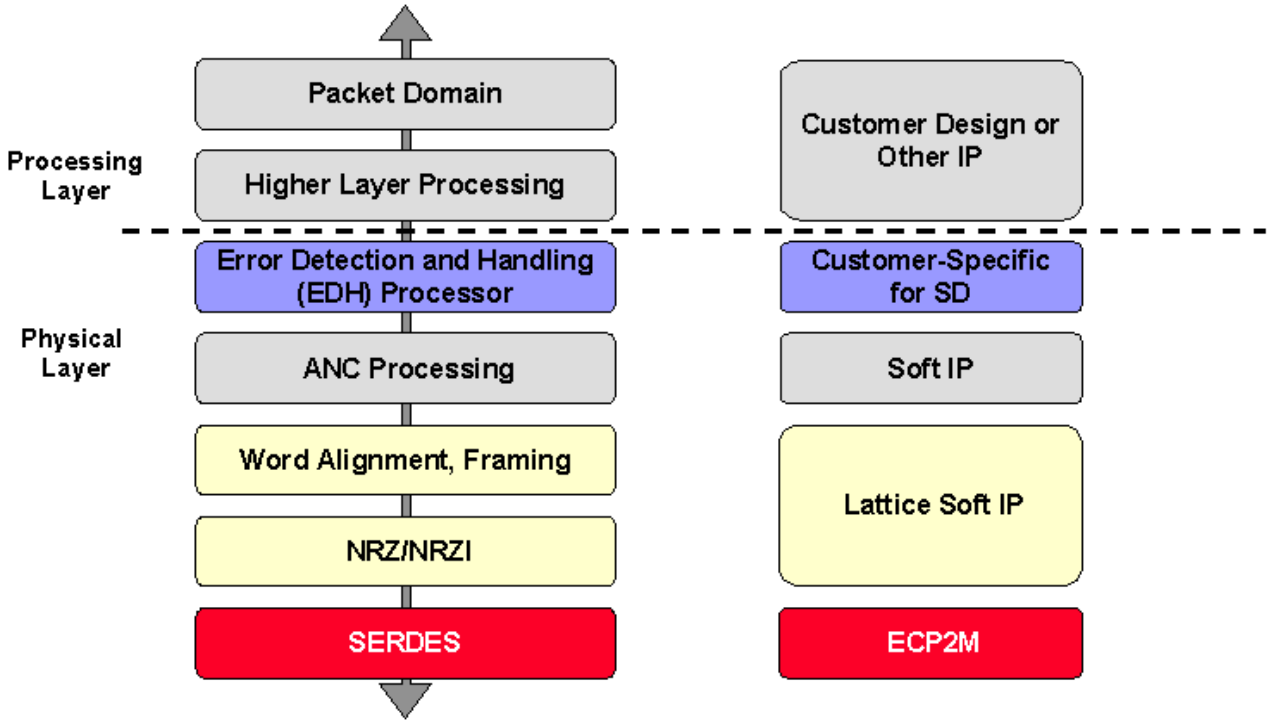
SDI is the most popular raw video link standard used in television broadcast studios and video production facilities. FPGAs (Field Programmable Gate Arrays) with SDI interface capability can be used for acquisition, mixing, storage, editing, processing, and format conversion applications. Many applications use FPGAs to acquire SDI data from one or more standard definition (SD) or high definition (HD) sources, perform simple processing and re-transmit the video data in SDI format. Such applications require an SDI PHY (physical layer) interface and some basic processing like a color space converter and frame buffer. FPGA devices can also be used as a bridge between SDI video sources and backplane protocols such as PCI Express or ethernet.

In an FPGA-based SDI solution, the physical interface portion is often the most challenging part of the solution. The Lattice Multi-Rate SDI PHY Layer IP core is a complete SDI PHY interface that connects to the high-speed SDI serial data on one side and formatted parallel data on the other side. It supports SMPTE standards 125M, 259M, 260M, 267M, 274M, 292M, 295M, and 296M and comprises high-speed serial I/Os (serializer/de-serializer or SerDes), SDI encoder, decoder, word alignment logic, CRC detection and checking logic, and rate detection logic. It is optimized to work with the LatticeECP2M/S embedded Physical Coding Sublayer (PCS) and SerDes, enabling a complete, single-chip solution ideally suited for a wide set of applications requiring high-performance, high-integration, and low-cost.

Below are a system block diagram of the Multi-Rate SDI PHY Layer IP core and an illustration of a video broadcast solution that can be implemented with the LatticeECP2M device and the core.



Top View, Multi-Rate SDI PHY Layer IP Core



SMPTE Protocol Stack for a Video Broadcast Solution

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Features

- Support for dynamic multi-rate SD-SDI/HD-SDI interfaces (SMPTE 259M [1] and 292M [2])
- Support for automatic Rx (receive) rate detection and dynamic Tx (transmit) rate selection
- Built-in SerDes programming for multi-rate support
- Support for multiple SD source formats: SMPTE 125M and sMPTE 267M (13.5 MHz only)
- Support for multiple HD source formats: SMPTE 260M [5], SMPTE 274M [6], SMPTE 295M [7], and SMPTE 296M [8])
- Word alignment and timing reference sequence (TRS) detection
- Field vertical blanking (vblank) and horizontal blanking (hblank) identification
- CRC computation, error checking, and insertion for HD
- Line number (LN) decoding and encoding for HD

Performance and Resource Utilization

Results for LatticeECP2M[1]

IPexpress User-Configurable Mode	SLICEs	LUTs	Registers	Tx f_{MAX} (MHz)	Rx f_{MAX} (MHz)
Rx/Tx	497	987	646	202	152
Tx only	122	224	229	227	n/a
Rx only	439	867	506	n/a	148

[1] Performance and utilization characteristics are generated using LFE2M-35E-6F672C with Lattice's ispLEVER 7.1 software. When using this IP core in a different density, package, speed, or grade within the LatticeECP2M family, performance and utilization may vary. The Multi-Rate SDI PHY Layer IP core is an IPexpress user-configurable core and can be used to generate any allowable configuration.

Evaluation Board

The Multi-Rate SDI PHY Layer IP core may be evaluated using the **LatticeECP2M SMPTE SDI Evaluation Board**.

Ordering Information

Part Numbers:
For LatticeECP2M: MR-SDI-PHY-PM-U1

To find out how to evaluate or purchase the Multi-Rate SDI PHY Layer IP core, please contact your **local Lattice Sales Office**.