Author: Yi Tian

ISL97646 Evaluation Board Application Manual

Description

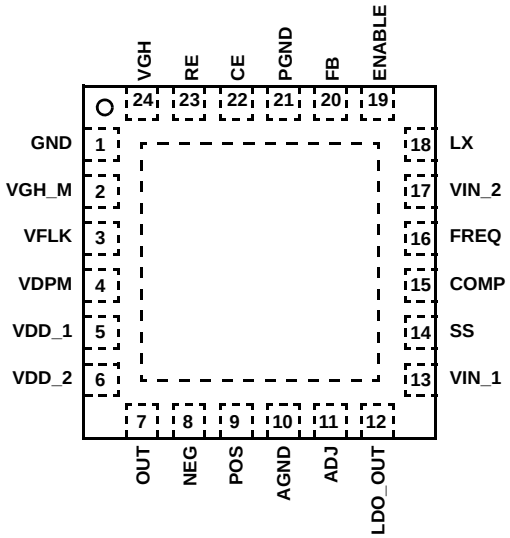
The ISL97646IRZ-EVALZ is an evaluation board for the ISL97646, which is a DC/DC voltage regulator for TFT-LCD displays with screen sizes up to 20". ISL97646 integrates a boost converter, a V_{ON} slice circuit, an LDO and a high performance V_{COM} amplifier. This evaluation board is designed to:

1. Deliver up to 0.8A current for AVDD supply to the source/column driver ICs
2. Generate different V_{ON} (gate high) and V_{OFF} (gate low)
3. Modulate VGH_M output for gate high voltage with desired delay time and discharge slope using the V_{ON} slice circuit
4. The high performance amplifier generates the LCD pixel common bias voltage (VCOM)
5. The LDO outputs up to 350mA for external digital circuitry

The ISL97646 evaluation board provides a dip switch that allows users to select either 650kHz or 1.2MHz and the enable signal to enable or disable the IC.

Pin Configuration

ISL97646
(24 LD 4x4 QFN)
TOP VIEW



Features

- A complete TFT-LCD PMIC evaluation platform for the ISL97646
- Input voltage: 2.7V to 5.5V
- Non-synchronous boost for AVDD supply
- V_{ON} and V_{OFF} charge pumps for gate driver IC supplies
- V_{ON} slice circuit for VGH_M
- LDO for external digital circuitry supply
- Op Amp follower for VCOM
- Layout Guidelines
- RoHS compliant

What is Needed

- The following instruments will be needed to perform testing:
  - Power supplies
  - DC Electronic load
  - Multimeters
  - Oscilloscope
  - Resistors
  - Cables and wires

Ordering Information

PART #	DESCRIPTION
ISL97646IRZ-EVALZ	Evaluation Board for ISL97646

Quick Setup Guide

Step 1: Connect the power supply between the headers of VIN and VIN_GND. The positive output of the power supply should be connected to the VIN header. Set the power supply voltage between 2.7V and 5.5V, and the current limit at 4A.

Step 2: Connect the positive and negative inputs of the Electronic load to the AVDD header and the AVDD_GND header, respectively. The load current should not exceed the maximum output current listed in Table 1.

Step 3: Set S1 towards the direction of the arrow in order to tie the FREQ pin to VIN, which will set 1.2MHz switching frequency; set S1 towards the reverse direction of the arrow to pull FREQ to ground with R16, to set the frequency to 650kHz.

Step 4: Set S2 towards the direction of the arrow in order to tie the ENABLE pin to VIN, which will enable the part; set S2 towards the reverse direction of the arrow in order to pull Enable to ground with R17, to disable the part.

Step 5: Connect pin 2 of JP4 to pin 3 of JP4 to enable LDO; connect pin 2 of JP4 to pin 1 of JP4 to disable LDO.

Step 6: Connect pin 2 of JP5 to pin 3 of JP5 to enable Gate Pulse Modulation (VGH_M); connect pin 2 of JP5 to pin 1 of JP5 to disable VGH_M.

Step 7: Connect the positive and negative inputs of the electronic load to the LDO_OUT header and the LDO_GND header, respectively.

Step 8: Connect the Electronic load between the headers of V_{ON} and Vin_GND. The positive input of the E-load should be connected to the V_{ON} header; the negative input of the E-load should be connected to Vin_GND. Connect the E-load between the headers of V_{OFF} and Vin_GND. The positive input of the E-load should be connected to Vin_GND header; the negative input of the E-load should be connected to V_{OFF}. Set the current values of the E-load. The values of V_{ON} and V_{OFF} at different loadings are shown in Table 2.

Step 9: Connect the header of V_{ON} to the VGH pin.

Step 10: Connect the input from the signal generator between the headers of VFLK and SGND. Select square waveform with an amplitude of 3.3V and a frequency of 50kHz.

Step 11: Connect the power supply between the headers of POS and SGND. Set the power supply voltage at the desired VCOM value.

Step 12: Make sure all the connections on the EVB are correct, then turn on the power supply and E-loads. The part will start to operate.

Maximum Boost Output Current

The MOSFET current limit is 2.6A. This limits the maximum output current that ISL97646 can drive. Table 1 shows the maximum output current I_{OMAX} at different input and output voltages.

TABLE 1. TYPICAL MAXIMUM OUTPUT CURRENT

V_{IN} (V)	V_{OUT} (V)	I_{OMAX} (mA)
3.3	8	800
3.3	12	480
5	8	1370
5	12	850

NOTES:

1. Table 1 shows typical maximum output current values for 1.2MHz switching frequency and 10µH inductor.
2. Maximum current values in actual application may vary with component variance.
3. Feedback compensation parameters and input and output capacitance of the boost may need to be modified to keep good stability with maximum peak inductor current of 2.6A.

Gate Pulse Modulator Timing Diagram

The ISL97646 evaluation board can generate a modulated VGH_M with a fixed power-on delay time, a discharging slope and a delay time to the falling edge of VFLK. The waveform of VGH_M is shown in Figure 1.

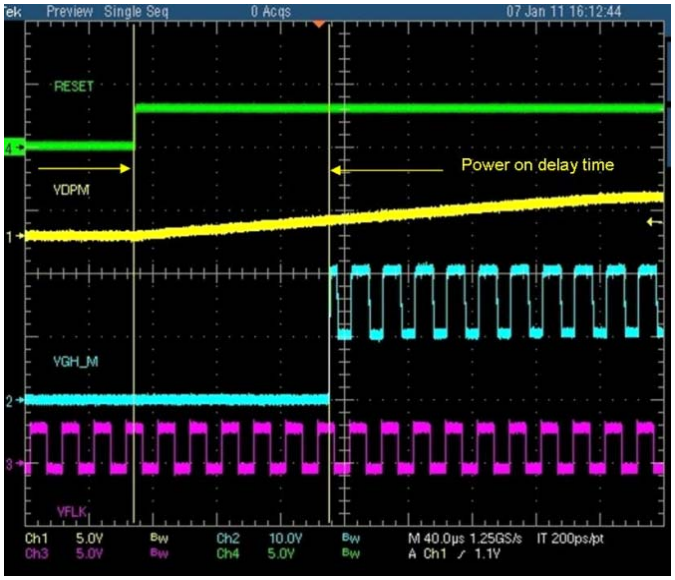


FIGURE 1. POWER ON DELAY TIME

LDO Output Voltages

The output voltage is adjusted by the connection of the ADJ pin. When ADJ is connected to ground, the output voltage is set to 3.3V; when ADJ pin is floating, the output voltage is set to 2.85V; and when ADJ pin is connected to LDO_OUT pin, the output voltage is set to 2.5V.

VON and VOFF at Different Loadings

The boost converter integrated in ISL97646 is capable of outputting up to 20V AVDD. This ISL97646 evaluation board generates VON and VOFF based on the output AVDD designed. Table 2 shows different values of VON and VOFF at different AVDD and different loadings for 1.2MHz switching frequency. By removing R18 and adding C24 and D3 into the circuit, the charge pump is able to deliver a VON higher than 2*AVDD.

Recommended Layout

The device performance, including efficiency, output noise, transient response and control loop stability, is dramatically affected by the PCB layout. PCB layout is critical, especially at high switching frequency.

Following are some general guidelines for layout:

1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{IN} and VDD bypass capacitors close to the pins.
3. Reduce the loop area with large AC amplitudes and fast slew rate.
4. The feedback network should sense the output voltage directly from the point of load, and should be placed to the IC and as far away from LX node as possible.
5. The power ground (PGND) and signal ground (SGND) pins should be connected at only one point at the exposed die plate, underneath the package.
6. The exposed die plate should be soldered to an equivalent area of metal on the PCB. This contact area should have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers, if available, to maximize thermal dissipation away from the IC.
7. To minimize the thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air.
8. A signal ground plane, separated from the power ground plane and connected to the power ground pins only at the exposed die plate, should be used for ground return connections for control circuit.
9. Minimize feedback input track lengths to avoid switching noise pick-up.

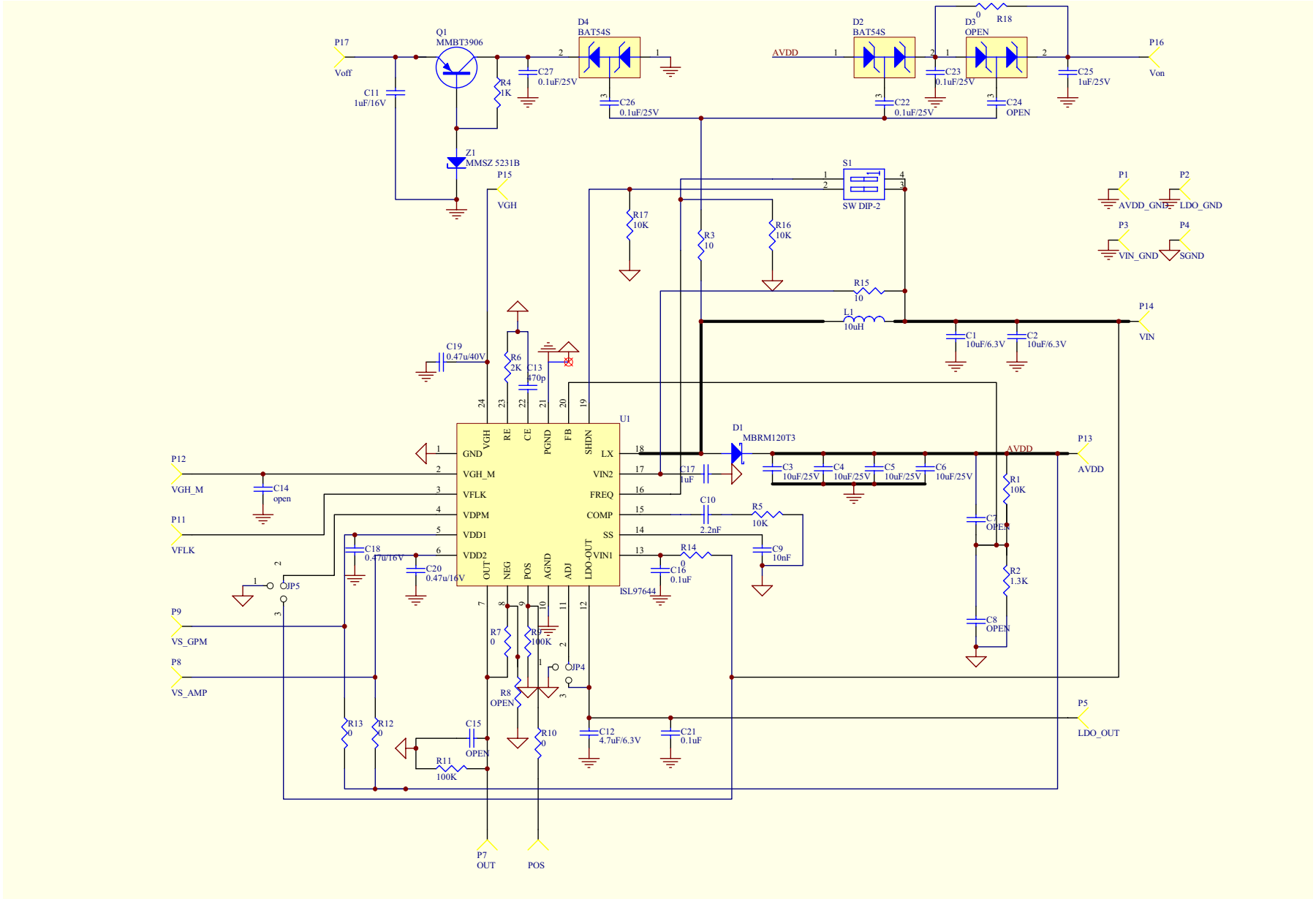
The EVB board layout shown on page 5 to page 7 is available to illustrate the proper layout implementation.

TABLE 2. TYPICAL VON AND VOFF FOR DIFFERENT LOADING

	VON (V)			VOFF (V)	
ILOADING	AVDD = 8V Single Stage	AVDD = 8V Two Stages	AVDD = 12V Single Stage	AVDD = 8V	AVDD = 12V
1mA	15.2	23.4	23.8	4.3	4.4
5mA	15.1	23.2	23.3	4.3	4.3
10mA	14.7	23.0	23.2	4.2	4.3

Evaluation Board Design

Schematic



Evaluation Board Layout

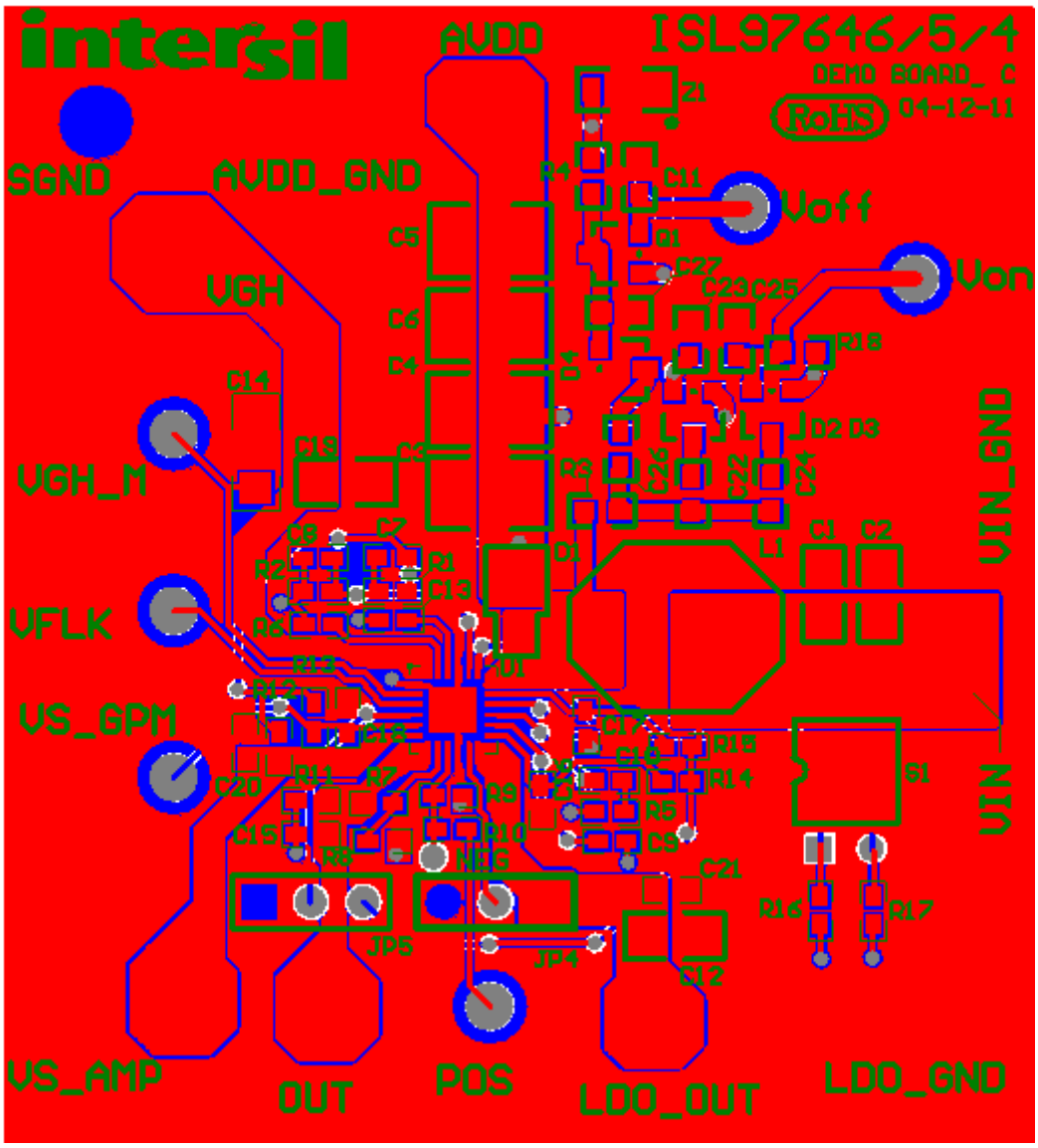


FIGURE 2. EVB ASSEMBLY LAYER

Evaluation Board Layout (Continued)

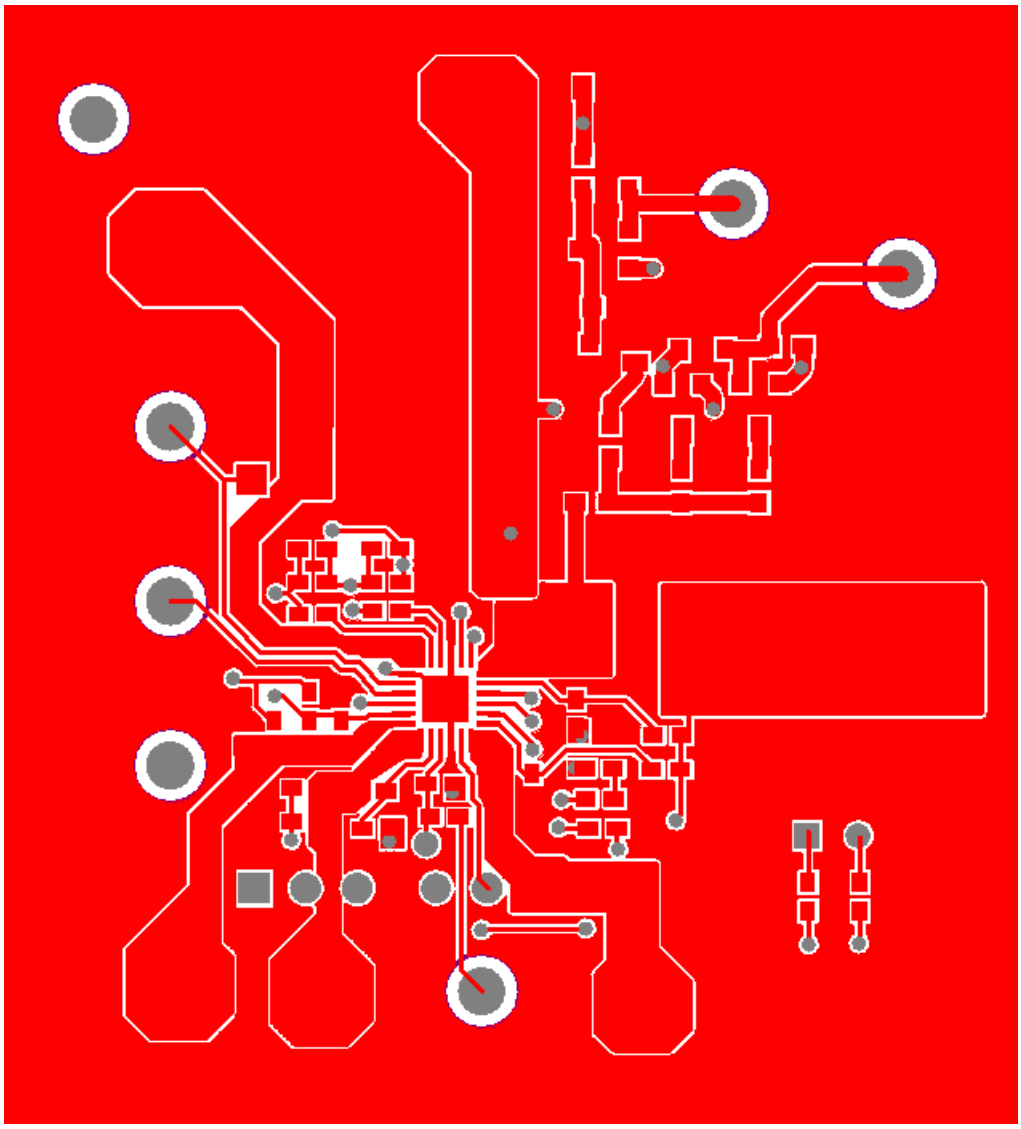


FIGURE 3. TOP LAYER

Evaluation Board Layout (Continued)

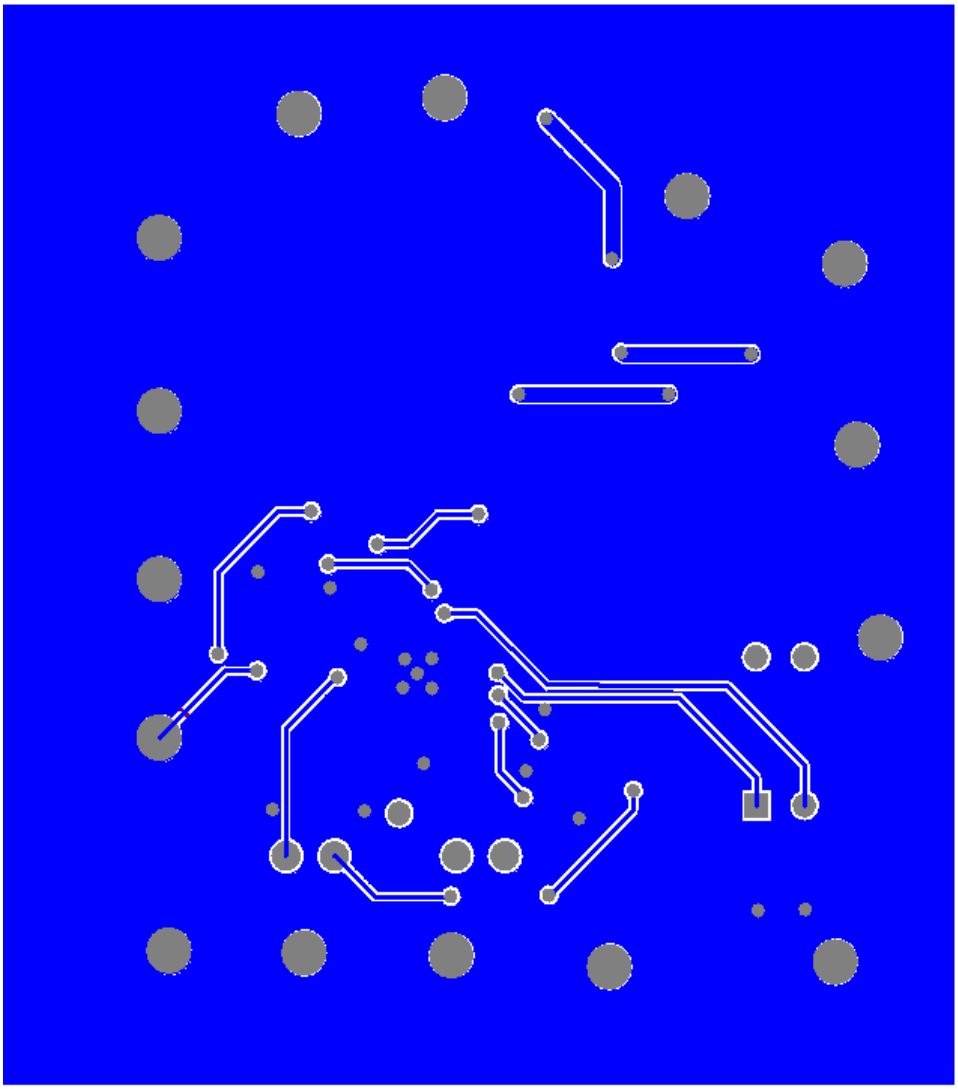


FIGURE 4. BOTTOM LAYER

Bill of Materials for ISL97646 Evaluation Board

PART TYPE	DESIGNATOR	FOOTPRINT
10k	R1	0603
1.3k	R2	0603
10	R3	0603
1k	R4	0603
10k	R5	0603
2k	R6	0603
0	R7	0603
OPEN	R8	0603
100k	R9	0603
0	R10	0603
100k	R11	0603
0	R12	0603
0	R13	0603
0	R14	0603
10	R15	0603
10k	R16	0603
10k	R17	0603
0	R18	0603
10µF/6.3V	C1	0805
10µF/6.3V	C2	0805
10µF/25V	C3	1210
10µF/25V	C4	1210
10µF/25V	C5	1210
10µF/25V	C6	1210
OPEN	C7	0603
OPEN	C8	0603
10nF/25V	C9	0603
2.2nF/25V	C10	0603
1µF/16V	C11	0603
4.7µF/6.3V	C12	0805
470pF	C13	0603
OPEN	C14	1206
OPEN	C15	0603
0.1µF/25V	C16	0603
1µF	C17	0603
0.47µF/16V	C18	0603
0.47µF/50V	C19	0805
0.47µF/16V	C20	0603
0.1µF/6.3V	C21	0603

Bill of Materials for ISL97646 Evaluation Board (Continued)

PART TYPE	DESIGNATOR	FOOTPRINT
0.1µF/25V	C22	0603
0.1µF/25V	C23	0603
OPEN	C24	0603
1µF/25V	C25	0603
0.1µF/25V	C26	0603
0.1µF/25V	C27	0603
1µF/16V	C28	0603
MBRM120T3	D1	Case457
BAT54S	D2	SOT-23
OPEN	D3	SOT-23
BAT54S	D4	SOT-23
ADJ JP	JP4	JUMPER-3PIN
VDPM JP	JP5	JUMPER-3PIN
10µH	L1	RLF7030
AVDD_GND	P1	POWERPOST
LDO_GND	P2	POWERPOST
VIN_GND	P3	POWERPOST
SGND	P4	POWERPOST
VDIV	P5	POWERPOST
POS	P6	POWERPOST
OUT	P7	POWERPOST
VS_AMP	P8	POWERPOST
VS_GPM	P9	POWERPOST
VFLK	P11	POWERPOST
VGH_M	P12	POWERPOST
AVDD	P13	POWERPOST
VIN	P14	POWERPOST
VGH	P15	POWERPOST
V_{ON}	P16	POWERPOST
V_{OFF}	P17	POWERPOST
MMBT3906	Q1	SOT-23
SW DIP-2	S1	DIP4
ISL97646	U1	24 LD 4X4 QFN
MMSZ 5233B	Z1	SOD-123