High-Performance Programmable Oscillators

Features

- Low-noise PLL for integrated crystal applications
- Differential Clock Output: re-configurable through I^2C
- Output frequency support from 15 MHz to 2.1 GHz
- Fractional N PLL with fully integrated VCO
- Works on an integrated fixed frequency crystal
- LVPECL, LVDS, HCSL, and CML output standards available
- Compatible with 3.3 V, 2.5 V, and 1.8 V supply
- 150 fs typical integrated jitter performance (12 kHz to 20 MHz frequency offsets) for outputs greater than 150 MHz
- VCXO functionality provided with tunable Total Pull Range (TPR) from ±50 ppm to ±275 ppm
- 8-pin LCC package 7.0 × 5.0 (CY2941x) or 5.0 × 3.2 (CY2942x) mm

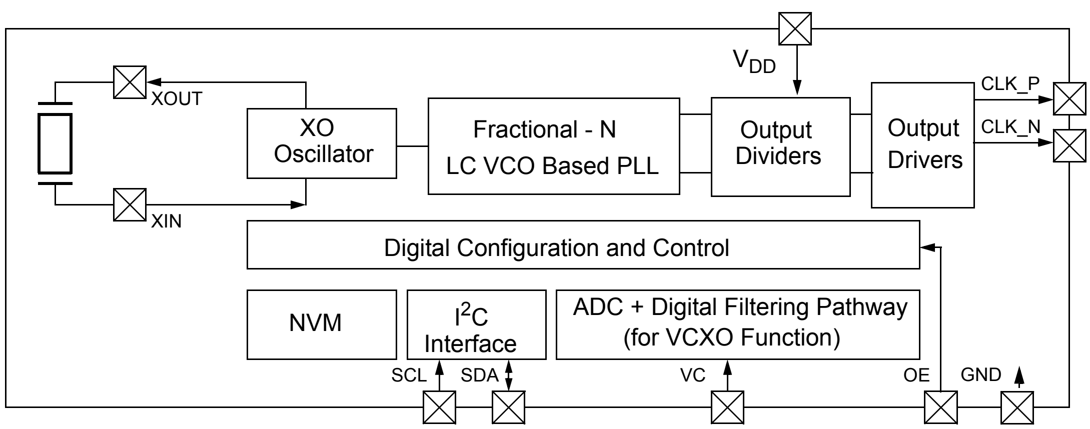
Functional Description

The CY2941x/CY2942x is a programmable PLL-based crystal oscillator solution with flexible output frequency options. It is field or factory-programmable for any output frequency between 15 MHz and 2.1 GHz. Other frequency options can be configured with the I^2C interface. Using advanced design technology, it provides excellent jitter performance across the entire output frequency range, working reliably at supply voltages from 1.8 V to 3.3 V for ambient temperatures from –40 °C to +105 °C. This makes it ideally suited for communications applications (for example, OTN, SONET/SDH, xDSL, GbE, networking, wireless infrastructure), test and instrumentation applications, and high-speed data converters. Additionally, the VCXO function enables use of the CY2941x/CY2942x series in applications requiring a clock source with voltage control, and in discrete clocking solutions for synchronous timing applications.

The CY2941x/CY2942x device configuration can be created using ClockWizard 2.1. For programming support, contact Cypress technical support or send an email to clocks@cypress.com.

For a complete list of related documentation, click here.

Logic Block Diagram



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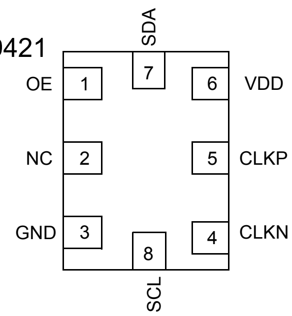
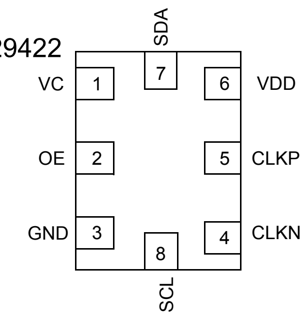
Pin Diagrams

CY29411, CY29421



CY29412, CY29422



Pin Description

Name	Pin Number	Description
CY29411/CY29421 (8-pin LCC)		
OE	1	Output Enable input
NC	2	Not connected
GND	3	Supply ground
CLKN	4	Complement clock output
CLKP	5	True clock output
V_{DD}	6	Power supply
SDA	7	Serial data input/output
SCL	8	Serial clock input for I^2C
CY29412/CY29422 (8-pin LCC)		
VC[1]	1	Input voltage for VCXO
OE	2	Output enable input
GND	3	Supply ground
CLKN	4	Complement clock output
CLKP	5	True clock output
V_{DD}	6	Power supply
SDA	7	Serial data input/output
SCL	8	Serial clock input for I^2C

Note

1. If VC is unused, do not leave it floating; connect it to VDD or GND.

Functional Overview

Programmable Features

Table 1. Programmable Features

Feature	Details
Frequency Tuning	Frequency for the PLL
	Oscillator tuning (load capacitance values)
Function	OE Polarity, I^2C Address
Power Supply	V_{DD} (1.8, 2.5, or 3.3 V)
VCXO	Enable/Disable VCXO
	Kv Polarity
	TPR
	Modulation Bandwidth
Output Standard	LVPECL, LVDS, HCSL, CML

Architecture Overview

The CY2941x/CY2942x devices are high-performance programmable PLL crystal oscillators supporting multiple functions and multiple output standards. The device has internal one-time programmable (OTP) nonvolatile memory (NVM) that can be partitioned into Common Device Configurations and Output frequency-related information (see Figure 2). The Common Device Configurations do not change with output frequency and consist of chip power supply, OE polarity, I^2C device address, input reference, output standard, and VCXO. The CY2941x/CY2942x devices also contain volatile memory (shown as “NVMCopy” in Figure 1) that stores an exact copy of the NVM at the release of reset on Power ON. The Chip settings depend on the contents of the volatile memory and the output frequency depends on the configurations stored in it, as explained in Figure 1. The volatile memory can be accessed through the I^2C bus and modified.

Figure 1. NVM and Volatile Memory Structure

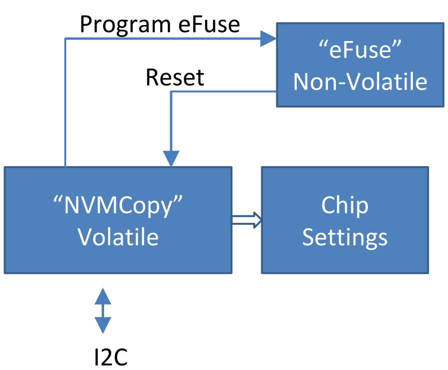
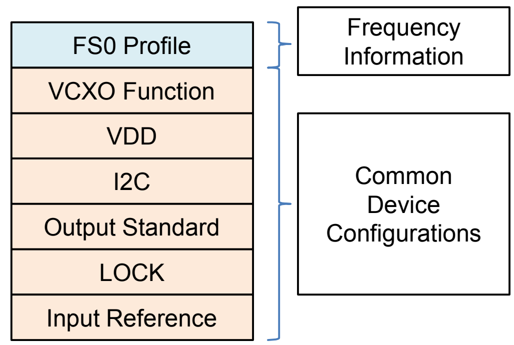


Figure 2 shows the conceptual internal memory structure that consists of Frequency Profile and Common Device Configuration settings.

Figure 2. Memory Structure



Description of Settings for the Memory Structure

- FS0: Contains frequency information
- VCXO Function: Contains parameters related to VCXO functionality, enable/disable, TPR, modulation bandwidth and Kv (Slope for VC vs. Frequency) information
- V_{DD}: 1.8-/2.5-/3.3-V range information
- I^2C address: I^2C address (programmable) information
- Output Standard: LVPECL, LVDS, HCSL or CML
- LOCK: 2-bit pattern to indicate NVM lock
- Input Reference: Information is Fixed, cannot be modified by the user

Internal State Diagram

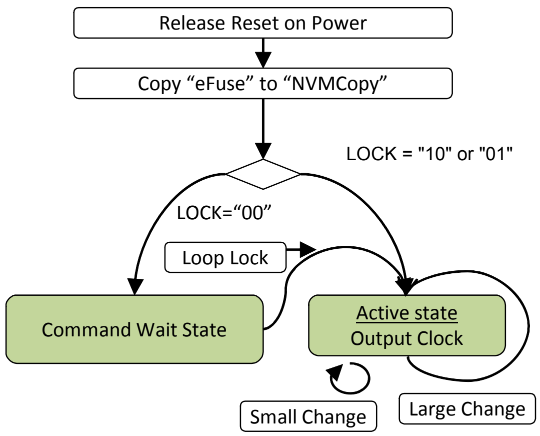
The CY2941x/CY2942x contains a state machine which controls the device behavior. The state machine loads the “eFuse” contents to “NVMCopy” after reset as indicated in the Figure 3 on page 5. The state machine enters one of the following states: “Command Wait state” or “Active state” according to the value of LOCK. In the “Command Wait state” state, user may access all the registers and read/write the “NVMCopy” contents. The following commands can be used in the “Command Wait state”:

The LOCK state is determined by a 2-bit pattern: 00, 01, 10, or 11. When the Power rail reaches a value within the specified range, the device comes out of the Reset state.

The blank device has LOCK=”00” (NVM not locked) in Figure 3 on page 5 so that it goes to the “Command Wait state” after coming out of Reset. The State machine will wait for the following commands:

- Write to volatile memory
- Program Non-Volatile memory (NVM)
- Loop Lock

Figure 3. State Diagram



When the LOCK is programmed to "10" or "01", the device will go to the “Active state” and the device will perform at the programmed frequency.

In the “Command Wait state”, you can configure the device with or without writing to the NVM. The use case scenarios are as follows:

- Test output frequency
  - Write to volatile memory and selectively write to NVM if needed
  - Proceed to Loop Lock can optionally be done for testing purpose

In the NVM locked state, the NVM cannot be reprogrammed. If needed, the output frequency may be changed using Large or Small change commands.

Small/Large Change

Small Change indicates that the frequency is changing within ±500 ppm. The frequency information will be loaded through I^2C and the output frequency will change without any glitch from its original frequency to the new frequency. For more information, see AC Electrical Specifications for LVPECL, LVDS, CML Outputs.

Large Change indicates that the frequency is changing more than ±500 ppm and is done through the I^2C interface.The device will recalibrate and reconfigure the PLL. The output will be stable after completion of this process.

Programming Support

The CY2941x/CY2942x is a software-configurable solution, in which Cypress provides programming software to users to configure the programmable features of the device based on their requirements.

Programmable OE Polarity

The CY2941x/CY2942x contains a bit for OE polarity setting (default is active low). You can choose active-high or active-low polarity for the OE function. The output will be disabled when OE is deasserted.

Programmable VCXO

The device incorporates a proprietary technique for modulating frequency by modifying the VCO frequency based on the VC control voltage. The pull profile is linear and accurate compared to pulling the crystal reference. Also, the VCXO characteristics are very stable and do not vary over temperature, supply voltage, or process variations.

Kv (Slope for frequency vs. VC), TPR VC bandwidth, and VCXO on/off are programmable.

Power Supply Sequencing

The CY2941x/CY2942x does not require any specific sequencing for startup. Startup requires a monotonic V_{DD} ramp specified in the datasheet. After the ramp up, V_{DD} has to be maintained within the limits specified for it in the Recommended Operating Conditions. Brownout detection and protection has to be implemented elsewhere in the system.

Other input signals can power up earlier or later than V_{DD}, there is no timing requirement for the input signals with reference to V_{DD}. The device will operate normally when all the input signals are settled to the configured state.

I^2C Interface

The CY2941x/CY2942x supports two-wire serial interface and I^2C in Fast Mode (400 kbps) and 7-bit addressing. The device address is programmable and is 55h by default. It supports single-byte access only. The first I^2C access to the device has to be 5 ms (minimum) after VDD reaches its minimum specified voltage.

Memory Map

Table 2. Common Configurations

Memory Address	Descriptions
50h–57h	Device configurations

Table 3. FS0: Frequency Configurations

Memory Address	Descriptions
10h	DIVO
11h	DIVO, DIVN_INT
12h	ICP,DIVN_INT, PLL_MODE
13h	DIVN_FRAC_L
14h	DIVN_FRAC_M
15h	DIVN_FRAC_H

Table 4. Misc information

Memory Address	Description
00h (Read only)	Device ID (= 51h)
D4h–D6h	User configurable information

The user must write all the contents created by the Configuration tool. Partial updates to the device is not allowed. Access to locations other than those described here may cause fatal error in device operation.

Absolute Maximum Ratings

Exceeding maximum ratings[2] may shorten the useful life of the device. User guidelines are not tested.

Supply voltage to ground potential ....–0.5 V to + 3.8 V

Input voltage ....–0.5 V to + 3.8 V

Storage temperature (non-condensing) ... –55 °C to +150 °C

Junction temperature .... –40 °C to +125 °C

Programming temperature .... 0 °C to +125 °C

Programming voltage ....2.5V ±0.1 V

Supply Current for eFuse Programming .... 50 mA

Data retention at T_J = 100 °C ....> 10 years

Maximum programming cycles 1

ESD HBM (JEDEC JS-001-2012) .... 2000 V

ESD MM (JEDEC JESD22-A115B) .... 200 V

ESD CDM (JEDEC JESD22-C101E) .... 400 V

Latch-up current .... ±140 mA

Recommended Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Core supply voltage, 1.8-V operating range, 1.8 V ± 5%	1.71	1.89	V
	Core supply voltage, 2.5-V operating range, 2.5 V ± 10%	2.25	2.75	
	Core supply voltage, 3.3-V operating range, 3.3 V ± 10%	2.97	3.63	
T_A	Ambient temperature	–40	+105	°C
UL-94	Flammability rating. V-0 at 1/8 in.	–	10	ppm
f_{RES}	Frequency resolution	–	2	ppb
$T_{PLLHOLD}$	PLL Hold Temperature Range	–	125	°C

DC Electrical Specifications

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current, LVPECL	V_{DD} = 3.3 V/2.5 V, 50 Ω to V_{TT} (V_{DD} – 2.0 V), with common mode current	–	93	106	mA
	Supply current, LVPECL	V_{DD} = 3.3 V/2.5 V, 50 Ω to V_{TT} (V_{DD} – 2.0 V), without common mode current[3]	–	81	94	
	Supply current, LVDS	V_{DD} = 3.3 V/2.5 V/1.8 V, 100 Ω between CLKP and CLKN	–	69	81	
	Supply current, HCSL	V_{DD} = 3.3 V/2.5 V/1.8 V, 33 Ω and 49.9 Ω to GND	–	80	93	
	Supply current, CML	V_{DD} = 3.3 V/2.5 V/1.8 V, 50 Ω to V_{DD}	–	73	86	
	Supply current, PLL only	V_{DD} = 3.3 V/2.5 V/1.8 V	–	59	70	
I_{IH}	Input high current	Logic input, Input = V_{DD}	–	30	50	µA
I_{IL}	Input low current	Logic input, Input = GND	–	30	50	µA
V_{IH}[4]	Input high voltage	OE, SCL, SDA logic level = 1	0.7 × V_{DD}	–	–	V
V_{IL}[4]	Input low voltage	OE, SCL, SDA logic level = 0	–	–	0.3 × V_{DD}	V
V_{IN}	Input voltage level	All input, relative to GND	–0.5	–	3.8	V
R_P	Internal pull-up resistance	OE, configured active High	–	200	–	kΩ
R_D	Internal pull-down resistance	OE, configured active Low	–	200	–	kΩ

Notes

2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.
3. In ClockWizard 2.1, setting the output standard to LVPECL2 configures the output to "LVPECL without common mode current". Refer to AN210253 for LVPECL terminations for different use case configurations.
4. I^2C operation applicable for V_{DD} of 1.8 V and 2.5 V only.

DC Specifications for LVDS Output

(V_{DD} = 1.8-V, 2.5-V, or 3.3-V range)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OCM}[5]	Output common-mode voltage	V_{DD} = 2.5-V or 3.3-V range	1.125	1.200	1.375	V
ΔV_{OCM}	Change in V_{OCM} between complementary output states	–	–	–	50	mV
I_{OZ}	Output leakage current	Output off, V_{OUT} = 0.75 V to 1.75 V	–20	–	20	µA

DC Specifications for LVPECL Output

(V_{DD} = 2.5-V or 3.3-V range, with common mode current)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage	R-term = 50 Ω to V_{TT} (V_{DD} – 2.0 V)	V_{DD} – 1.165	–	V_{DD} – 0.800	V
V_{OL}	Output low voltage	R-term = 50 Ω to V_{TT} (V_{DD} – 2.0 V)	V_{DD} – 2.0	–	V_{DD} – 1.55	V

DC Specifications for CML Output

(V_{DD} = 1.8-V, 2.5-V or 3.3-V range)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage	R-term = 50 Ω to V_{DD}	V_{DD} – 0.085	V_{DD} – 0.01	V_{DD}	V
V_{OL}	Output low voltage	R-term = 50 Ω to V_{DD}	V_{DD} – 0.6	V_{DD} – 0.4	V_{DD} – 0.32	V

DC Specifications for HCSL Output

(V_{DD} = 1.8-V, 2.5-V, or 3.3-V range)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{MAX}[6]	Max output high voltage	Measurement taken from single-ended waveform	–	–	1150	mV
V_{MIN}[6]	Min output low voltage	Measurement taken from single-ended waveform	–300	–	–	mV
V_{OHDIFF}	Differential output high voltage	Measurement taken from differential waveform	150	–	–	mV
V_{OLDIFF}	Differential output low voltage	Measurement taken from differential waveform	–	–	–150	mV
V_{CROSS}[6]	Absolute crossing point voltage	Measurement taken from single-ended waveform	250	–	600	mV
$V_{CROSSDELTA}$[6]	Variation of V_{CROSS} over all rising clock edges	Measurement taken from single-ended waveform	–	–	140	mV

Notes
5. Requires external AC coupling for V_{DD} = 1.8-V range, as indicated in Figure 9.
6. Parameters are guaranteed by design and characterization. Not 100% tested in production.

V_{CXO} Specific Parameters

Parameter [7]	Description	Condition	Min	Typ	Max	Units
TPR	Total Pull Range	VC range 0.1 × V_{DD} to 0.9 × V_{DD}	±50	–	±275	ppm
K_{BSL}	Best-fit Straight Line (BSL) linearity	Deviation from BSL line	–5	–	5	%
K_{INC}	Incremental linearity	Kv slope deviation	–10	–	10	%
K_{BW}	Bandwidth of Kv modulation	Programmable	5	10	20	kHz
K_{RANGE}	Voltage range	Permissible voltage range	0	–	V_{DD}	V
V_{CTYP}	Nominal center voltage	VC control voltage	–	0.5 × V_{DD}	–	V
R_{VCIN}[8]	Input resistance for VC	–	5	–	–	MΩ
V_{RANGE}	Input voltage range	Linearity guaranteed range	0.1 × V_{DD}	–	0.9 × V_{DD}	V

Notes
7. Parameters are guaranteed by design and characterization. Not 100% tested in production.
8. RVCIN is 100% tested.

AC Electrical Specifications for LVPECL, LVDS, CML Outputs

(V_{DD} = 3.3 V and 2.5 V for LVPECL, with common mode current, and V_{DD} = 3.3 V, 2.5 V, and 1.8 V for LVDS and CML outputs)

Parameter[9]	Description	Details/Conditions	Min	Typ	Max	Unit
f_{OUT}	Clock Output Frequency	LVPECL, CML, LVDS output standards	15	–	2100	MHz
t_{RF}	LVPECL Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for PECL outputs.	–	–	350	ps
	CML Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for CML outputs.	–	–	350	ps
	LVDS Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for LVDS outputs.	–	–	350	ps
t_{ODC}	Output Duty Cycle	Measured at differential 50% level, 156.25 MHz.	45	50	55	%
V_P	LVDS output differential peak	15 MHz to 700 MHz	247	–	454	mV
V_P	LVDS output differential peak	700 MHz to 2100 MHz	150	–	454	mV
ΔV_P	Change in VP between complementary output states	–	–	–	50	mV
V_P	LVPECL output differential peak	f_{OUT} = 15 MHz to 325 MHz	450	–	–	mV
V_P		f_{OUT} = 325 MHz to 700 MHz	350	–	–	mV
V_P		f_{OUT} = 700 MHz to 2100 MHz	250	–	–	mv
V_P	CML output differential peak	f_{OUT} = 15 MHz to 700 MHz	250	–	600	mV
V_P	CML output differential peak	f_{OUT} = 700 MHz to 2100 MHz	200	–	600	mV
t_{CCJ}	Cycle to Cycle Jitter	pk, measured at differential signal, 156.25 MHz, over 10k cycles, 100 MHz–130 MHz crystal	–	–	50	ps
t_{PJ}	Period Jitter	pk-pk, measured at differential signal, 156.25 MHz, over 10k cycles, 100 MHz–130 MHz crystal	–	–	50	ps
J_{RMS}	RMS Phase Jitter	f_{OUT} = 156.25 MHz, 12 kHz–20 MHz offset, non-VCXO mode	–	150	250	fs
Non-VCXO Mode						
PN1k	Phase Noise, 1 kHz Offset	100-130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	-113	dBc/Hz
PN10k	Phase Noise, 10 kHz Offset	100-130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	-127	dBc/Hz
PN100k	Phase Noise, 100 kHz Offset	100-130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	-135	dBc/Hz
PN1M	Phase Noise, 1MHz Offset	100-130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	-144	dBc/Hz
PN10M	Phase Noise, 10 MHz Offset	100-130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	–152	dBc/Hz
PN-SPUR	Spur	At frequency offsets equal to and greater than the update rate of the PLL	–	–	–65	dBc/Hz

Note

9. Parameters are guaranteed by design and characterization. Not 100% tested in production.

AC Electrical Specifications for HCSL Output

Parameter [10]	Description	Test Conditions	Min	Typ	Max	Units
f_{OUT}	Output frequency	HCSL	15	–	700	MHz
E_R	Rising edge rate	Measured taken from differential waveform, –150 mV to +150 mV	0.6	–	5.7[11]	V/ns
E_F	Falling edge rate	Measured taken from differential waveform, –150 mV to +150 mV	0.6	–	5.7[11]	V/ns
t_{STABLE}	Time before voltage ring back (VRB) is allowed	Measured taken from differential waveform, –150 mV to +150 mV	500	–	–	ps
$R\text{-}F_{\_MATCHING}$	Rise-Fall matching	Measured taken from single-ended waveform, rising edge rate to falling edge rate matching, 100 MHz	–100	–	100	ps
t_{DC}	Output duty cycle	Measured taken from differential waveform, f_{OUT} = 100 MHz	45	–	55	%
t_{CCJ}	Cycle to Cycle Jitter	Measured taken from differential waveform, 100 MHz	–	–	50	ps
$J_{RMSPCIE}$	Random jitter, PCIE Specification 3.0	100 MHz–130 MHz crystal	–	–	1	ps (RMS)

Timing Parameters

Parameter [10]	Description	Min	Max	Unit
t_{PU}	Supply ramp time (0.5 V to $V_{DD(min)}$). Power ramp must be monotonic.	0.01	3000	ms
t_{WAKEUP}	Time from minimum specified power supply to < ±0.1 ppm accurate output frequency clock	–	10	ms
t_{OEEN}	Time from OE edge to output enable	–	2.5	ms
t_{OEDIS}	Time for OE edge to output disable	–	10	µs
t_{FSMALL}	Frequency change time for small trigger (≤ ±500 ppm)	–	400	µs
t_{FLARGE}	Frequency change time for large trigger (> ±500 ppm)	–	2.5	ms

Notes
10. Parameters are guaranteed by design and characterization. Not 100% tested in production.
11. Edge rates are higher than 4 V/ns due to jitter performance requirements.

Phase Jitter Characteristics

12 kHz to 20 MHz Integration Bandwidth

Parameter[12]	Description	Condition	Min	Typ	Max	Units
Non VCXO functionality						
J_{RMS}	RMS jitter	F_{OUT} = 644.53 MHz	–	110	–	fs
J_{RMS}	RMS jitter	F_{OUT} = 622.08 MHz	–	120	–	fs
J_{RMS}	RMS jitter	F_{OUT} = 156.25 MHz	–	145	–	fs
J_{RMS}	RMS jitter	F_{OUT} = 2.105 GHz	–	145	–	fs
Modulation bandwidth = 10 kHz, V_{DD} = 3.3 V, F_{OUT} = 622.08 MHz						
J_{RMS}	RMS jitter	TPR = 50 ppm, Kv = 37.9 ppm/V	–	151	–	fs
J_{RMS}	RMS jitter	TPR = 155 ppm, Kv = 117.4 ppm/V	–	158	–	fs
J_{RMS}	RMS jitter	TPR = 275 ppm, Kv = 208.3 ppm/V	–	170	–	fs
Modulation bandwidth = 10 kHz, V_{DD} = 2.5 V, F_{OUT} = 622.08 MHz						
J_{RMS}	RMS jitter	TPR = 50 ppm, Kv = 50 ppm/V	–	152	–	fs
J_{RMS}	RMS jitter	TPR = 155 ppm, Kv = 155 ppm/V	–	160	–	fs
J_{RMS}	RMS jitter	TPR = 275 ppm, Kv = 275 ppm/V	–	175	–	fs
Modulation bandwidth = 10 kHz, V_{DD} = 1.8 V, F_{OUT} = 622.08 MHz						
J_{RMS}	RMS jitter	TPR = 50 ppm, Kv = 69.4 ppm/V	–	153	–	fs
J_{RMS}	RMS jitter	TPR = 155 ppm, Kv = 215.3 ppm/V	–	166	–	fs
J_{RMS}	RMS jitter	TPR = 275 ppm, Kv = 381.9 ppm/V	–	190	–	fs

I^2C Bus Timing Specifications

Parameter [12, 13]	Description	Min	Typ	Max	Units
f_{SCL}	SCL clock frequency	–	–	400	kHz
$t_{HD:STA}$	Hold time START condition	0.6	–	–	µs
t_{LOW}	Low period of SCL	1.3	–	–	µs
t_{HIGH}	High period of SCL	0.6	–	–	µs
$t_{SU:STA}$	Setup time for a repeated START condition	0.6	–	–	µs
$t_{HD:DAT}$	Data hold time	0	–	–	µs
$t_{SU:DAT}$	Data setup time	100	–	–	ns
t_R	Rise time	–	–	300	ns
t_F	Fall time	–	–	300	ns
$t_{SU:STO}$	Setup time for STOP condition	0.6	–	–	µs
t_{BUF}	Bus-free time between STOP and START conditions	1.3	–	–	µs

Notes
12. Parameters are guaranteed by design and characterization. Not 100% tested in production.
13. I^2C operation applicable for V_{DD} of 1.8 V and 2.5 V only.

Frequency Stability

Parameter	Description	Test Conditions	Min	Typ	Max	Units
$f_{TOLERANCE}$	Frequency Tolerance	V_{DD} = min to max, T_A = +25 °C	–20	–	+20	ppm
f_{TC}	Temperature Characteristics	V_{DD} = min to max, T_A = –40 °C to +85 °C	–20	–	+20	ppm
f_{TC}	Temperature Characteristics	V_{DD} = min to max, T_A = –40 °C to +105 °C	–30	–	+30	ppm
f_{AGE}	Frequency Aging		–5	–	+5	ppm/year

Voltage and Timing Definitions

Figure 4. Differential Output Definitions

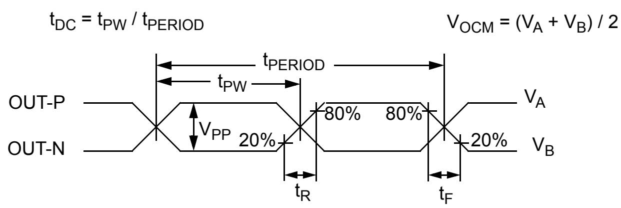


Figure 5. Output Enable/Disable Timing

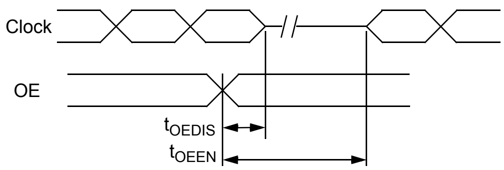


Figure 6. Power Ramp and PLL Lock Time

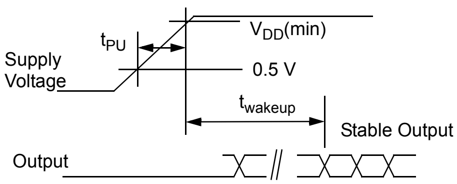


Figure 7. Output Termination Circuit

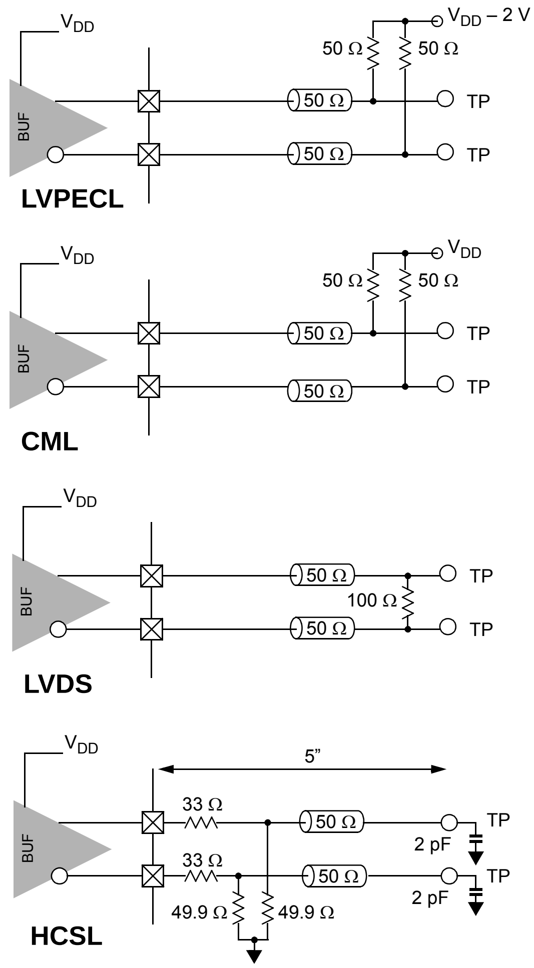
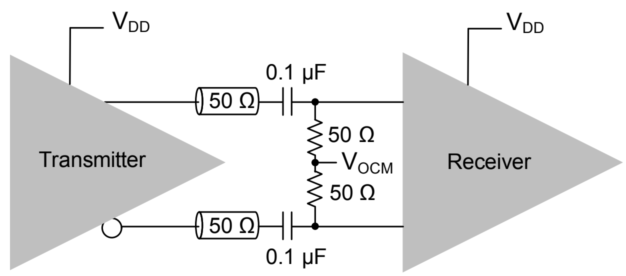


Figure 8. LVDS Termination for 1.8 V[14]



Note

14. The termination circuit shown in this figure is specific to the LVDS output standard for V_{DD} =1.8-V operation. This needs AC coupling (100-nF series capacitor). The 50-ohm termination resistors along with the bias voltage (V_{OCM}) is required to be set at the destination circuit as shown in the figure.

Figure 9. HCSL: Single-ended Measurement Points for Absolute Crossing Point

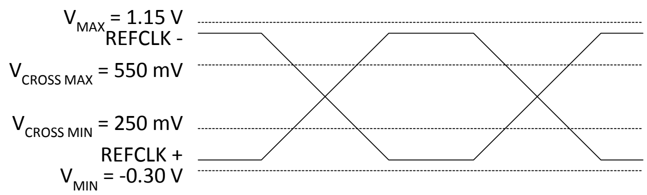


Figure 10. HCSL: Single-ended Measurement Points for Delta Crossing Point

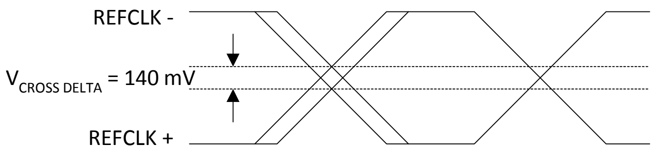


Figure 11. HCSL: Differential Measurement Points for Rise and Fall Time

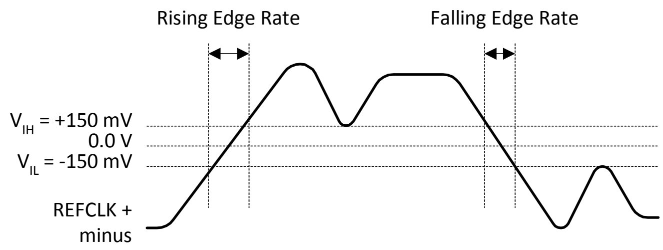


Figure 12. HCSL: Differential Measurement Points for Ringback

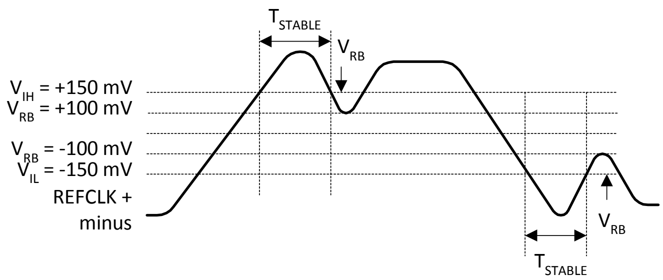
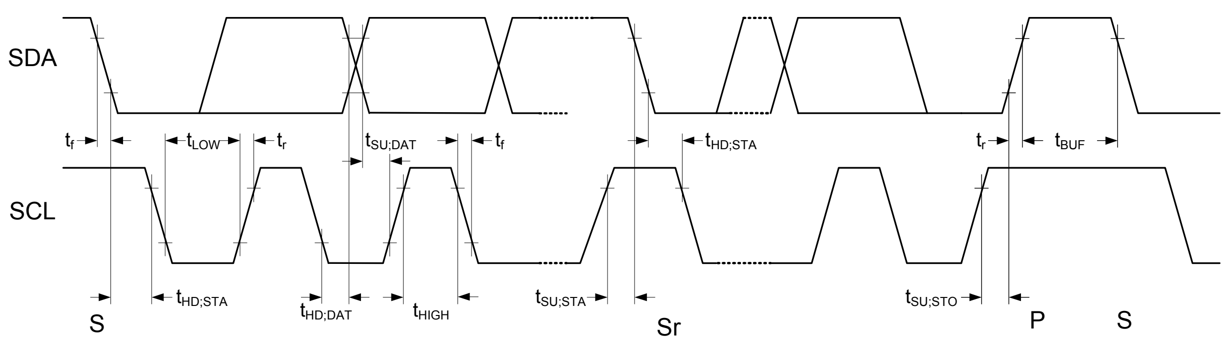


Figure 13. I²C Bus Timing Specifications



Phase Noise Plots

Figure 14. Typical Phase Noise at 156.25 MHz (12 kHz–20 MHz)

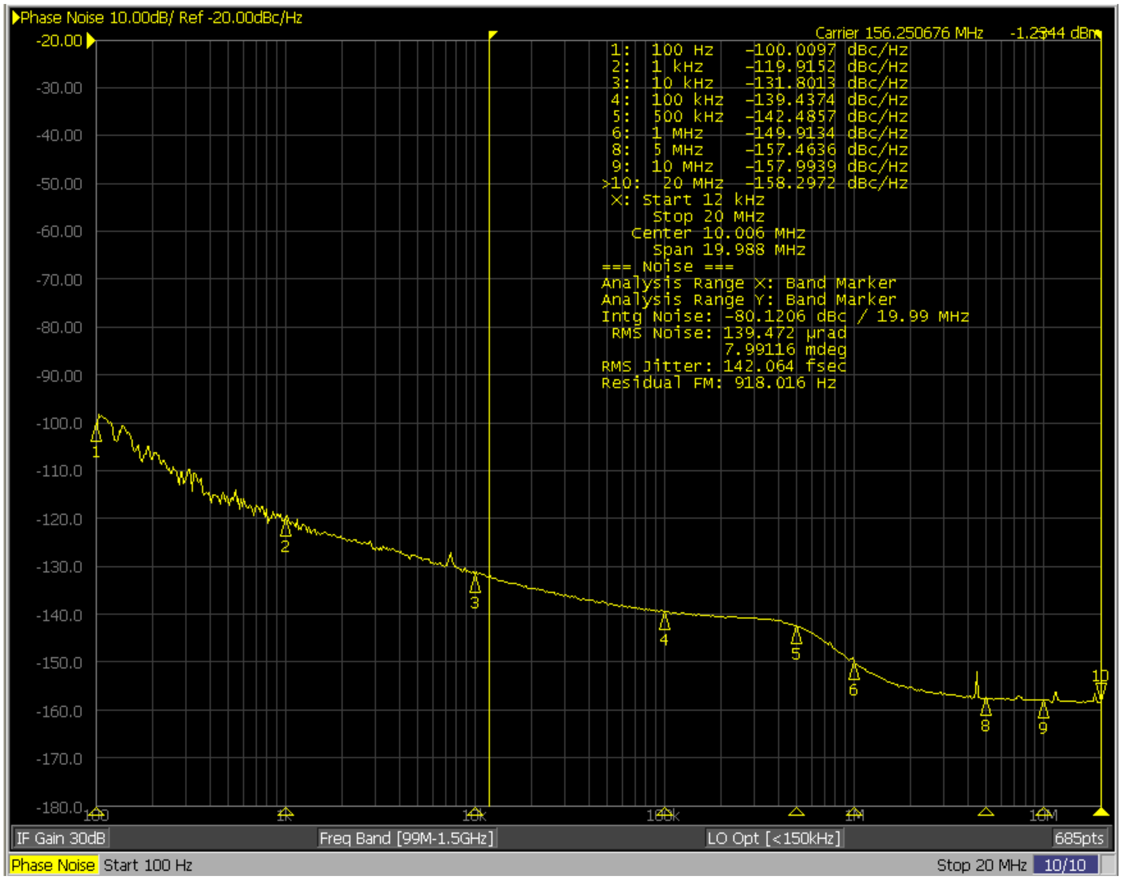


Figure 15. Typical Phase Noise at 622.08 MHz (12 kHz–20 MHz)

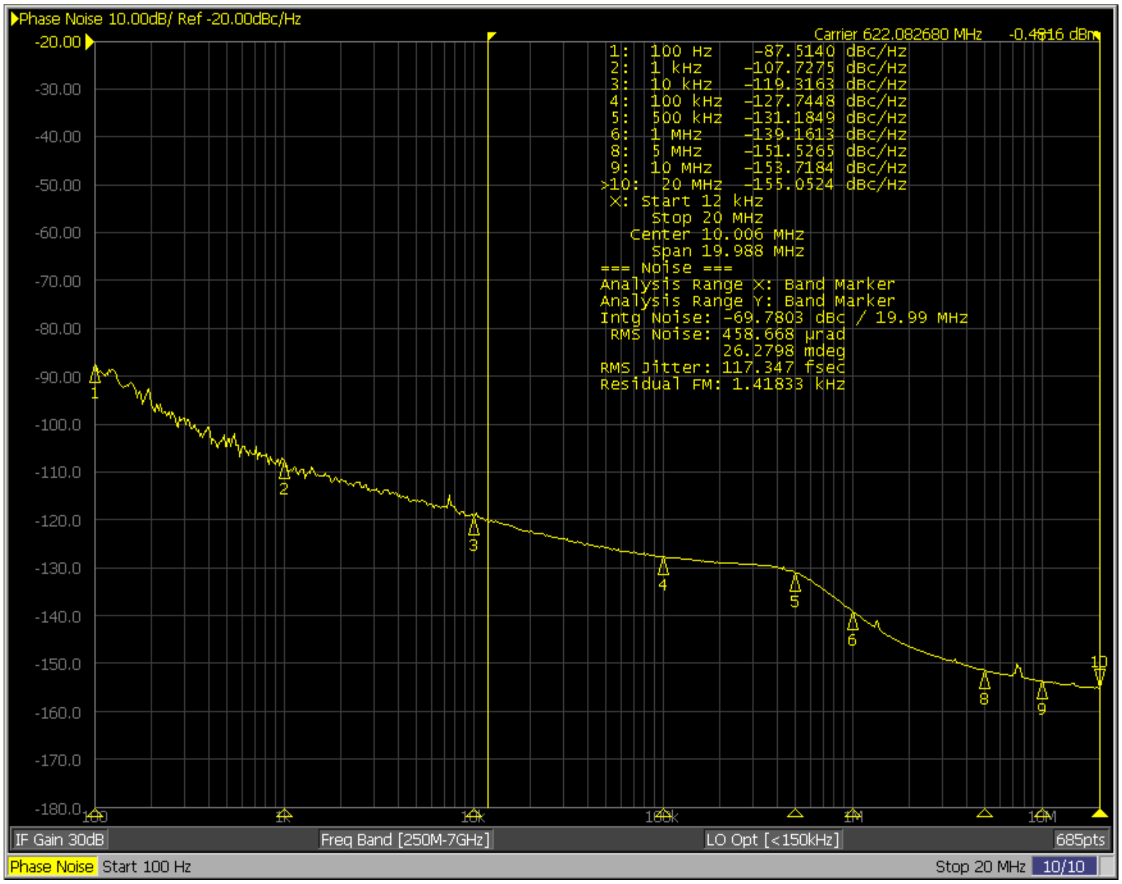
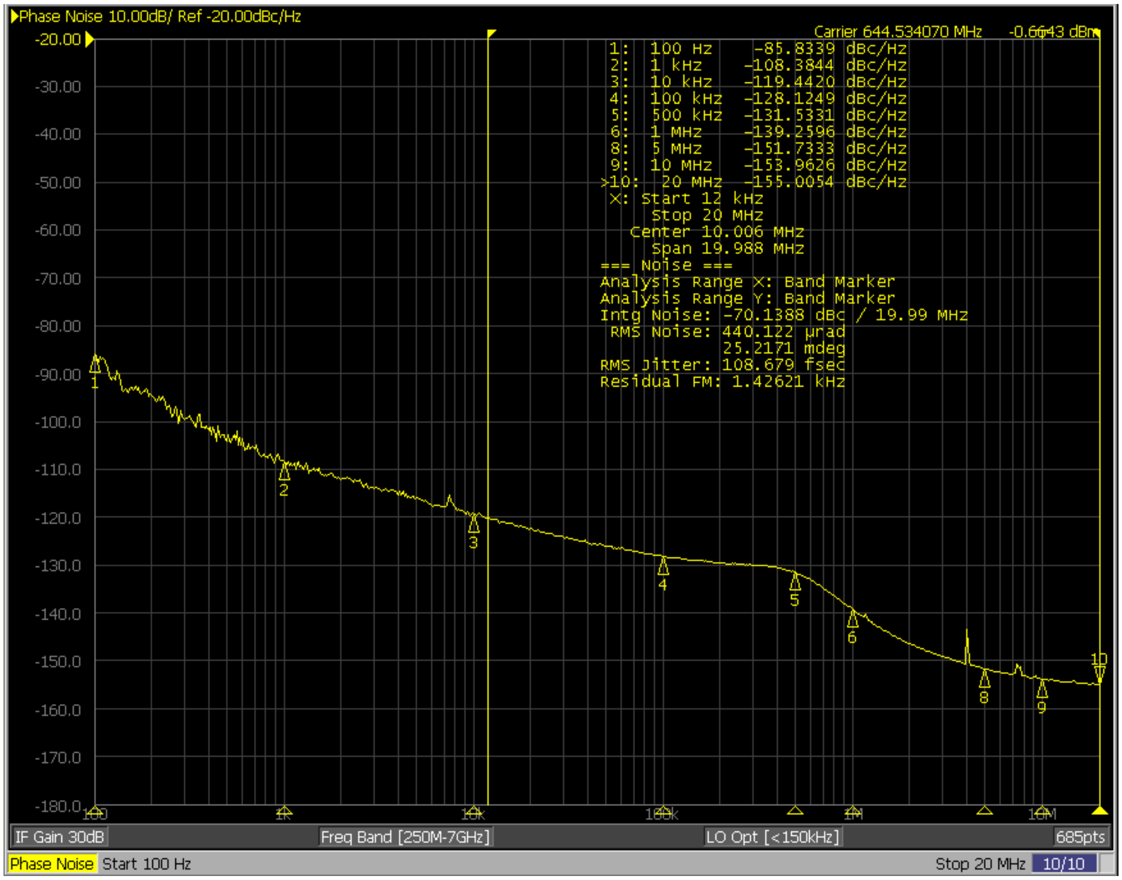


Figure 16. Typical Phase Noise at 644.53 MHz (12 kHz–20 MHz)



Ordering Information

Ordering Code	Configuration	Package Description	Product Flow
CY29411FLXIT	Field-programmable	8-pin LCC 7.0 × 5.0 mm – Tape and Reel	Industrial, –40 °C to +105 °C
CY29411LXIxxxT	Factory-configured[15]	8-pin LCC 7.0 × 5.0 mm – Tape and Reel	Industrial, –40 °C to +105 °C
CY29412FLXIT	Field-programmable	8-pin LCC 7.0 × 5.0 mm – Tape and Reel	Industrial, –40 °C to +105 °C
CY29412LXIxxxT	Factory-configured[15]	8-pin LCC 7.0 × 5.0 mm – Tape and Reel	Industrial, –40 °C to +105 °C
CY29421FLXIT	Field-programmable	8-pin LCC 5.0 × 3.2 mm – Tape and Reel	Industrial, –40 °C to +105 °C
CY29421LXIxxxT	Factory-configured[15]	8-pin LCC 5.0 × 3.2 mm – Tape and Reel	Industrial, –40 °C to +105 °C
CY29422FLXIT	Field-programmable	8-pin LCC 5.0 × 3.2 mm – Tape and Reel	Industrial, –40 °C to +105 °C
CY29422LXIxxxT	Factory-configured[15]	8-pin LCC 5.0 × 3.2 mm – Tape and Reel	Industrial, –40 °C to +105 °C

Ordering Code Definitions

CY 294xx X - LXI xxx T

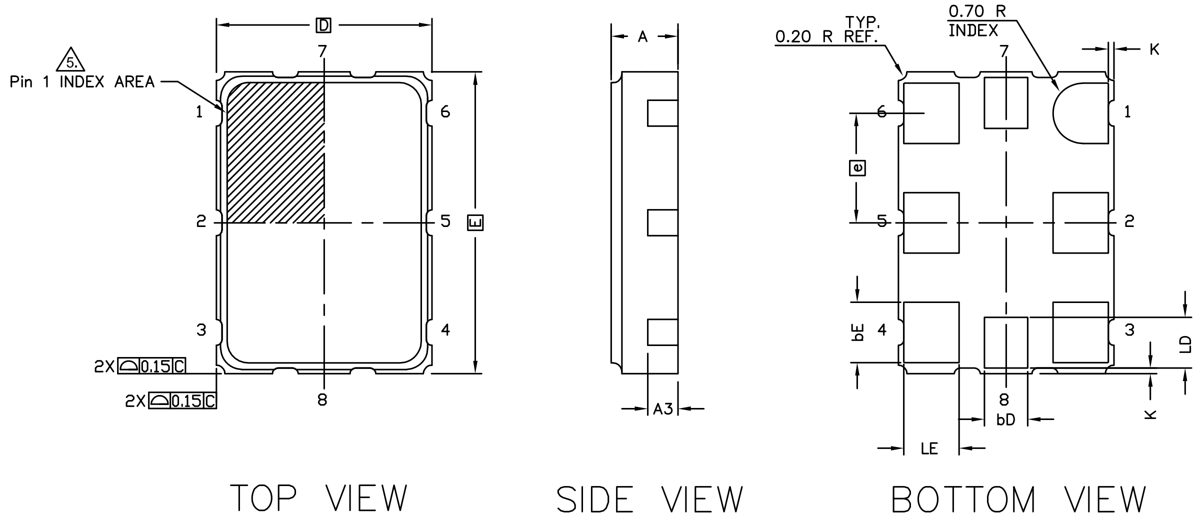
- T = Tape and Reel, Blank = Bulk
- xxx: Customer Part Configuration Code
- LXI: Package Type: LX(LCC), Pb-Free: X and Industrial: I
- X: Configuration: F = Field Programmable, Blank = Factory Configured
- 294xx: Part Number: 294xx = 29412 or 29422
- CY: Company ID: CY = Cypress

Note

15. These are factory-programmed customer-specific part numbers. Contact your local Cypress FAE or sales representative for more information.

Package Diagrams

Figure 17. 8-pin Ceramlc LCC (5.0 × 7.0 × 1.75 mm) Package Outline, 002-10174



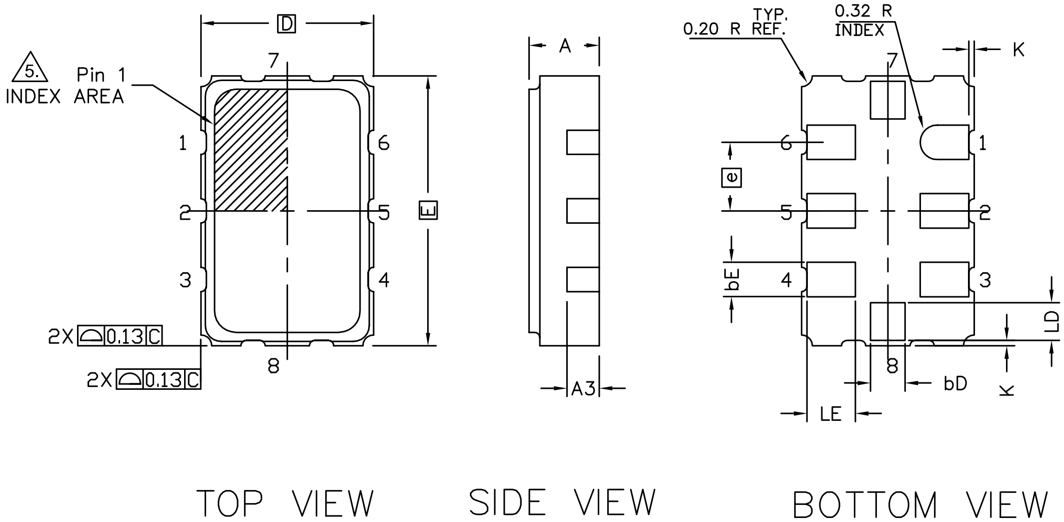
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	1.65	-	1.75
A3	0.70 REF		
D	5.00 BSC		
E	7.00 BSC		
bD	1.00		
bE	1.40		
LD	1.18		
LE	1.28		
K	0.13		
e	2.54 BSC		
N	8		
ND	1		
NE	3		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. ND IS THE NUMBER OF TERMINALS ON "D" DIMENSION.
4. NE IS THE NUMBER OF TERMINALS ON "E" DIMENSION.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.

002-10174 *A

Figure 18. 8-pin Ceramlc LCC (3.2 × 5.0 × 1.45 mm) Package Outline, 002-10273



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	1.35	-	1.45
A3	0.60 REF		
D	3.20 BSC		
E	5.00 BSC		
bD	0.64		
bE	0.64		
LD	0.70		
LE	0.90		
K	0.10		
e	1.27 BSC		
N	8		
ND	1		
NE	3		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. ND IS THE NUMBER OF TERMINALS ON "D" DIMENSION.
4. NE IS THE NUMBER OF TERMINALS ON "E" DIMENSION.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.

002-10273 *A

Acronyms

Table 5. Acronyms Used in this Document

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
BCL	best-fit straight line
CML	current mode logic
DC	direct current
ESD	electrostatic discharge
FS	frequency select
HCSL	high-speed current steering logic
I^2C	inter-integrated circuit
JEDEC	Joint Electron Device Engineering Council
LDO	low dropout (regulator)
LVCMOS	low voltage complementary metal oxide semiconductor
LVDS	low-voltage differential signals
LVPECL	low-voltage positive emitter-coupled logic
NVM	non-volatile memory
OE	output enable
PLL	phase-locked loop
POR	power-on reset
PSoC®	Programmable System-on-Chip
QFN	quad flat no-lead
RMS	root mean square
SCL	serial I^2C clock
SDA	serial I^2C data
VCXO	voltage controlled crystal oscillator
VRB	voltage ring back
XTAL	crystal
OTP	one time programmable

Document Conventions

Units of Measure

Table 6. Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
fs	femtoseconds
GHz	gigahertz
kΩ	kilohms
kHz	kilohertz
MHz	megahertz
MΩ	megaohms
µA	microamperes
µm	micrometer
µs	microseconds
µW	microwatts
mA	milliamperes
mm	millimeter
mΩ	milliohms
ms	milliseconds
mV	millivolts
nH	nanohenry
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
ps	picoseconds
ppm	parts per million
ppb	parts per billion
V	volts

Document History Page

Document Title: CY2941x/CY2942x, High-Performance Programmable Oscillators Document Number: 001-97768				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*C	5320399	07/18/2016	MGPL	Changed status from Preliminary to Final.
*D	5429121	09/07/2016	MGPL	Updated Absolute Maximum Ratings: Added “Supply Current for eFuse Programming”. Replaced “≥ 2000 V” with “2000 V” in value corresponding to “ESD HBM”. Replaced “> 200 V” with “200 V” in value corresponding to “ESD MM”. Replaced “>500V” with “400 V” in value corresponding to “ESD CDM”. Updated to new template.
*E	5518357	11/15/2016	MGPL/ PSR	Added Figure 8.
*F	5613574	02/03/2017	PSR	Added links to ClockWizard 2.1 and technical support, and added reference to related documentation in Functional Description. Updated LVPECL specs in DC Electrical Specifications. Added note clarifying voltage range in AC Electrical Specifications for LVPECL, LVDS, CML Outputs. Updated Ordering Information.
*G	5682054	04/03/2017	PSR	Updated the template. Deleted VDDO references. Added Clock Tree Services to Sales, Solutions, and Legal Information.

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