MCIMX53SMD Board Hardware User's Guide

IMX53SMDHUG
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1. Introduction

The MCIMX53SMD Board Hardware User's Guide is a user manual that describes the design and usage of the MCIMX53SMD board, which is a printed circuit board (PCB) based on Freescale Semiconductor's i.MX53 Applications Processor (AP). This guide specifies the basic architecture of the MCIMX53SMD board and explains the design and purpose of each component of the board. It also tells how developers can use the MCIMX53SMD board in their various development works.

1.1. MCIMX53SMD Board Overview

The MCIMX53SMD board is an i.MX53 platform that provides many widely used features of the i.MX53 Applications Processor in a tablet package. Being a complete development platform, the MCIMX53SMD board has a design structure that is almost similar to the more complex i.MX53 platforms. This helps developers to port code developed on the MCIMX53SMD board to other boards with minimal effort. Developers can use the MCIMX53SMD board to test the features of the i.MX53 Applications Processor, before investing a large amount of money or resources in more specific designs. **Figure 1-1** shows an MCIMX53SMD board with a debug card and a display.

Figure 1-1. MCIMX53SMD Board with a Debug Card and a Display

The different components of the MCIMX53SMD board are listed in **Table 1-1**.

Component	Description
Processor	Freescale Applications Processor – MCIMX535DVV1B/ MCIMX535DVV1C
DRAM memory	Micron 8 GB DDR3 SDRAM – MT41J128M16HA-125
PMIC	Dialog Semiconductor – DA9053
DCDC/charger	Maxim – MAX17085B

Mass storage	One SD/MMC/SDIO card connector
	8/32 GB SSD SATA
	4 MB SPI-NOR Flash
	8 GB eMMC
Video output	40-pin VGA Dock
	19-pin Mini-HDMI connector
	Two 30-pin LVDS connectors
USB	Two high speed (HS) USB 2.0 Standard-A host connectors
	Micro-B OTG connectors
Audio connectors	3.5 mm Stereo Headphone output
	Mono-Microphone input on board
	Two 1W at 8Ω speakers
Power connectors	15V connector
Debug connectors	9-pin D-Sub Debug UART connector
	RJ-45 connector for 10/100 Base-T
	20-pin Standard ARM JTAG connector
Peripheral	WiFi/BT card
	GPS module
	ZigBee
	5M-pixel camera sensor
Sensor	eCOMPASS
	Accelerometer
	Light sensor
Expansion header	120-pin header (populated) to support the optional WVGA and WQVGA LCD display daughter cards (orderable)
User interface buttons	Power, Reset, Vol+, and Vol- buttons
	Electrode touch keypad
Indicators	Six status LEDs, for example, external power, WiFi, and debug
Li-ION battery connector	5-pin header for Li-ION battery
Coin cell	Connection point for 2-pin coin cell required in RTC operation
PCB	200 mm x 166 mm, 8-layer board

Table 1-1. MCIMX53SMD Board Components

1.2. MCIMX53SMD Board Kit Contents

The MCIMX53SMD board comes with the following items:

- MCIMX53SMD main board
- MCIMX53SMD debug board
- Power supply (100/240V input, 15V 3A output)
- 3-cell Li-ion Battery and Charger (will be available in Q4, 2011)
- HDMI to HDMI cable
- Quick Start guide
- DVD, MCIMX53SMD, i.MX53 Getting Started

2. List of Acronyms

The acronyms used in this document are listed in Table 2-1.

Acronym	Used For
AC97	Audio Codec ‘97
CMC	Common Mode Choke
CODEC	Compression/Decompression
DDR	Double Data Rate
DNP	Do Not Populate
HDMI	High Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Integrated Interchip Sound
IC	Integrated Circuit
IDE	Integrated Debug Environment
LAN	Local Area Network
QSB	Quick Start Board
LCD	Liquid Crystal Display
LPDDR2	Low Power DDR2
MMC	Multi Media Card
PMIC	Power Management Companion IC
RMII	Reduced Media Independent Interface
RTC	Real-Time Clock
SDRAM	Synchronous Dynamic Random Access Memory
SD	Secure Digital
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
ULPI	UTMI Low Pin Interface
USB	Universal Serial Bus
UTMI	Universal Transceiver Macrocell Interface
WDOG	Watch Dog
WLAN	Wireless LAN

Table 2-1. List of Acronyms

3. Specifications

3.1. i.MX53 Applications Processor

The i.MX53 processor is based on ARM Cortex-A8™ Platform, which has the following features:

- MMU, L1 Instruction and L1 Data Cache
- Unified L2 cache
- Target frequency of the core (including Neon, VFPv3, and L1 Cache) is 1-1.2 GHz; target frequency of the MCIMX53SMD platform is 1 GHz
- Neon coprocessor (SIMD Media Processing Architecture) and Vector Floating Point (VFP-Lite) coprocessor supporting VFPv3
- TrustZone

The memory system of the processor consists of the following components:

- Level 1 Cache:
  - Instruction (32 Kbyte)
  - Data (32 Kbyte)
- Level 2 Cache:
  - Unified instruction and data (256 Kbyte)
- Level 2 (internal) memory:
  - Boot ROM, including HAB (64 Kbyte)
  - Internal multimedia/shared, fast access RAM (128 Kbyte)
  - Secure/non-secure RAM (16 Kbyte)
- External memory interfaces:
  - 16/32-bit DDR2-800, LV-DDR2-800 or DDR3-800 up to 2 Gbyte
  - 32 bit LPDDR2
  - 8/16-bit NAND SLC/MLC Flash, up to 66 MHz, 4/8/14/16-bit ECC
  - 16-bit NOR Flash. All WEIMv2 pins are muxed on other interfaces (data with NFC pins). I/O muxing logic selects WEIMv2 port, as primary muxing at system boot.
  - 16-bit SRAM, cellular RAM
  - Samsung One NANDTM and managed NAND including eMMC up to rev 4.4 (in muxed I/O mode)

The i.MX53 processor system is built around the following system-on-chip (SoC) interfaces:

- 64-bit AMBA AXI v1.0 bus: Used by ARM platform, multimedia accelerators (such as, VPU, IPU, GPU3D, GPU2D) and the external memory controller (EXTMC) operating at 200 MHz.
- 32-bit AMBA AHB 2.0 bus: Used by the rest of the bus master peripherals operating at 133 MHz.
- 32-bit IP bus: Peripheral bus used for control (and slow data traffic) of the most system peripheral devices operating at 66 MHz.

The i.MX53 processor makes use of dedicated hardware accelerators to achieve state-of-the-art multimedia performance. The use of hardware accelerators provides both high performance and low power consumption while freeing up the CPU core for other tasks.

The i.MX53 processor incorporates the following hardware accelerators:

- VPU, version 3: Video processing unit
- GPU3D: 3D graphics processing unit, OpenGL ES 2.0, version 3, 33 Htri/s, 200 Mpix/s, and 800 Mpix/s z-plane performance, 256 KB RAM memory.
- GPU2D: 2D graphics accelerator, OpenVG 1.1, version 1, 200 Mpix/s performance.
- IPU, version 3M: Image processing unit

- ASRC: Asynchronous sample rate converter

The i.MX53 processor includes the following interfaces to external devices:

NOTE

Not all the interfaces are available simultaneously depending on I/O multiplexer configuration.

- Hard disk drives:
  - PATA, up to U-DMA mode 5, 100 MByte/s
  - SATA II, 1.5 Gbps
- Displays:
  - Five interfaces: Total rate of all interfaces is up to 180 Mpixels/s, 24 bpp. Up to two interfaces may be active as once.
  - Two parallel 24-bit display ports: The primary port is up to 165 Mpix/s (for example, UXGA at 60 Hz).
  - LVDS serial ports: One dual channel port up to 165 Mpix/s or two independent single channel ports up to 85 MP/s (for example, WXGA at 60 Hz) each.
  - TV-out/VGA port up to 150 Mpix/s (for example, 1080p60).
- Camera sensors:
  - Two parallel 20-bit camera ports. Primary up to 180-MHz peak clock frequency and secondary up to 120-MHz peak clock frequency.
- Expansion cards:
  - Four SD/MMC card ports: Three supporting 416 Mbps (8-bit interface) and one enhanced port supporting 832 Mbps (8-bit, eMMC 4.4)
- USB
  - HS USB 2.0 OTG (up to 480 Mbps), with integrated HS USB PHY
  - Three USB 2.0 (480 Mbps) hosts:
    - High-speed host with integrated on-chip high speed PHY
    - Two high-speed hosts for external HS/FS transceivers through ULPI/serial, support IC-USB
- Miscellaneous interfaces:
  - One-wire (OWIRE) port
  - Three I2S/SSI/AC97 ports, supporting up to 1.4 Mbps, each connected to audio multiplexer (AUDMUX) providing four external ports.
  - Five UART RS232 ports, up to 4.0 Mbps each. One supports eight-wire and the other four support four-wire.
  - Two high speed enhanced CSPI (ECSPI) ports and one CSPI port
  - Three I2C ports, supporting 400 kbps
  - Fast Ethernet controller, IEEE1588 V1 compliant, 10/100 Mbps
  - Two controller area network (FlexCAN) interfaces, 1 Mbps each
  - Sony Philips Digital Interface (SPDIF), Rx and Tx
  - Enhanced serial audio interface (ESAI), up to 1.4 Mbps each channel
  - Key pad port (KPP)
  - Two pulse-width modulators (PWM)
  - GPIO with interrupt capabilities
  - Secure JTAG controller (SJC)

The system supports efficient and smart power control and clocking:

- Supporting DVFS (Dynamic Voltage and Frequency Scaling) and DPTC (Dynamic Process and Temperature Compensation) techniques for low power modes.

- Power gating SRPG (State Retention Power Gating) for ARM core and Neon
- Support for various levels of system power modes
- Flexible clock gating control scheme
- On-chip temperature monitor
- On-chip oscillator amplifier supporting 32.768 kHZ external crystal
- On-chip LDO voltage regulators for PLLs

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, and so on)
- Secure JTAG controller (SJC): Protecting JTAC from debug port attacks by regulating or blocking the access to the system debug features.
- Secure real-time clock (SRTC): Tamper resistant RTC with dedicated power domain and mechanism to detect voltage and clock glitches.
- Real-time integrity checker, version 3 (RTICv3): RTIC type 1, enhanced with SHA-256 engine
- SAHARAv4 Lite: Cryptographic accelerator that includes true random number generator (TRNG)
- Security controller, version 2 (SCCv2): Improved SCC with AES engine, secure/nonsecure RAM and support for multiple keys as well as TZ/non-TZ separation.
- Central Security Unit (CSU): Enhancement for the IIM (IC Identification Module). CSU is configured during boot and by eFUSEs and determines the security level operation mode as well as the TrustZone (TZ) policy.
- Advanced High Assurance BOOT (A-HAB): HAB with the next embedded enhancements: SHA-256, 2046-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

3.2. DDR3 DRAM Memory

The MCIMX53SMD board uses four 2-Gigabit DDR3 SDRAM ICs manufactured by Micron for a total onboard RAM memory of 1 GB. The SDRAM data width for each IC is 16 bits. The chips are arranged in pairs and they are controlled by the two chip select pins to form 32-bit words for the i.MX53 CPU. The On Die Termination (ODT) functionality has been implemented on the board. In addition, the board provides the ability to separate the I/O Voltage Supply from the main SDRAM Voltage Supply, if desired.

3.3. Dialog DA9053 PMIC

The DA9053 device is a small (7 x 7 mm, 0.5 mm pitch) 169 ball VFBGA that provides nearly all power supply functions for the MCIMX53SMD board. The DA9053 PMIC enhances the functionality of the MCIMX53SMD board by providing the following features:

- Power Supply resources:
    - 12 Low Drop Out (LDO) regulators
        - One for internal PMIC purposes only (LDOCORE)
        - One for charging optional back up coin cell
        - 10 for platform needs
    - Four DC/DC Buck Converters (three with DVS)
        - One for the ARM Core supply (VBUCKCORE)
        - One for the Peripheral Core supply (VBUCKPRO)
        - One for the external SDRAM memory (VBUCKMEM)
        - One for the internal cache memory (VBUCKPERI)
    - One White LED driver and boost converter
- Li-ION battery charger
- Resistive touch screen interface

- Expansion Port Card ID detect
- Wall voltage supply with over-voltage protection
- One HS-I2C interface
- External LDO regulator enable

3.4. Max17085B DCDC and Charger

The MAX17085B is an all-in-one notebook power solution that comprises of a multi-cell battery charger, dual fixed output Quick-PWM step-down controllers, and dual keep-alive linear regulators:

- One multi-cell battery charger
- Two DC/DC Buck Converters
  - One for the 3.3V supply
  - One for the 5V supply
- Two Low Drop Out (LDO) regulators
  - One for the 3.3V supply
  - One for the 5V supply

3.5. Mini-HDMI Connector (J25)

The mini-HDMI connector is used as HDMI output of MCIMX53SMD board. The power source for the HDMI Bridge SiI9022 is DCDC_3V3_BB, and the power source for mini-HDMI connector is DCDC_5V_BB.

3.6. SD Card Slot (J13)

The SD Card slot is a 5-in-1 SD/MMC connector that acts as memory media slot. The power source for the SD Card Slot is the auxiliary DCDC buck (DCDC_3V3_BB). The SD Card slot can be configured as the boot source with an alternate boot option setting. It can also be configured for either SD or MMC card operation (see the Boot Mode Operations and Selections section). The SD Card Slot supports full 4-bit parallel data transfers and can support SDIO cards (such as, WiFi and BT) designed to fit in a standard SD card slot.

3.7. SATA Connector (J5)

The SATA connector provides a means to connect an external SSD SATA drive to the MCIMX53SMD board. Power for the SATA drive needs to be supplied by SATA_5V and SATA_3V3. The developer can use boot configure to boot the SATA drive.

3.8. VGA Dock (J131)

A Dock with VGA signal is on the MCIMX53SMD board. VGA is the output that comes directly from the i.MX53 processor with minimum external components required. Power for the TVE module of the i.MX53 processor is supplied by VLDO7 of the PMIC and is set to 2.75V. If VGA output is not desired, the PMIC can be programmed to turn off VLDO7 to conserve power. The VGA output supports a variety of video formats up to 150 Megapixels per second. Level shifters are required on the Horizontal and Vertical Synchronization signals as well as the VGA I2C communications signals in order to meet VGA specifications. Meanwhile, Audio LINEIN and LINEOUT are supported on the Dock. The Audio LINEIN and LINEOUT are from SGTL5000 on MCIMX53SMD board. Another feature on Dock is USB.

3.9. LVDS Video Output (J28, J29)

The LVDS module of the i.MX53 processor is connected to two 30-pin LVDS connectors. Both connectors are pinned out on the MCIMX53SMD board, though the i.MX53 processor is capable of outputting to two separate LVDS displays. The pin outs on the LVDS connector match the optional cable and 10” HannStar LVDS display

(both can be purchased from Freescale). The single LVDS connector will support video formats up to 165 Megapixels per second. The power source for the LVDS module is a switchable output of the VBUCKPERI DCDC converter. This rail is shared with the SATA module and the USB module. If these modules are not used, the PMIC can be programmed to turn off power to these three modules, without affecting the 2.5V supplies to other portions of the i.MX53 processor.

3.10. Ethernet (on Debug Board)

The i.MX53 processor Fast Ethernet Module outputs RMII formatted signals to an external Ethernet PHY. The processor is capable of 10/100 Base-T speeds. The MCIMX53SMD board uses the SMSC LAN8720A Ethernet Transceiver in a QFN-24 package. The Ethernet IC is powered by a 3.3V supply from DCDC_3V3_BB. The output of the Ethernet PHY is connected to the debug board.

3.11. Dual USB Host Connector (J31, J32)

The USB module of the i.MX53 processor provides a high speed USB PHY that is connected to a USB HUB (USB2514). Two of the USB ports are dedicated to USB HOST. Both jacks receive 5V power from DCDC_5V through a power monitor that can be controlled by software.

3.12. Micro-B USB Device Connector (J34)

The micro USB connector is connected to the USB OTG PHY on the i.MX53 processer and supports full OTG function.

3.13. Audio Input/Output (P1/J130/CON1)

Analog audio input and output are provided by Freescale's Low Power Stereo Codec, SGTL5000. The audio codec is connected to the i.MX53 processor through four-wire I2S communications, utilizing the AUDMUX5 port of the processor. The audio codec's Headphone Amp provides up to 58 mW output to 16Ω headphones at a typical SNR of 98 dB and THD+N of -86 dB. Typical power consumption is 11.6 mW. In addition, the audio codec can perform several enhancements to the output, including virtual surround, added bass, and three different types of equalization. The Microphone Input module of the Stereo Codec is also used, while the microphone is applied on the MCIMX53SMD board. A Headphone Jack (J130) and Speaker Connector (CON1) are on the MCIMX53SMD board. A 3.5 mm Headphone with plug-in detect is supported. Two speakers with 8Ω impedance rating and 1W power rating are attached through a power amplifier (TS4984IQT).

3.14. 15V Power Connector (J35)

A 2.0 mm x 6.5 mm barrel connector is used which should fit standard DC Plugs with an inner dimension of 2.1 mm and an outer dimension of 5.5 mm. If a secondary power supply is used, it should not supply more than 15V power at 3A output. If the PMIC senses too high voltage at the connector input, it will turn off to protect the MCIMX53SMD board. If a Wall Power Supply is connected to the MCIMX53SMD board, the red 15V power LED indicator will light.

3.15. Mini-PCIe Connector (J15, J18)

Two mini-PCIe connectors are on the MCIMX53SMD board. One for 3G modem, the other is for WiFi/BT. The MCIMX53SMD board provides just a standard mini-PCIe slot for 3G Modem. So, the developers can use a 3G Modem of their choice. For the WiFI/BT module, the MCIMX53SMD board uses the module based on the Atheros. The module pin map is not compatible with the standard mini-PCIe. Therefore, care must be taken to plug the module to the right mini-PCIe slot.

3.16. CMOS Sensor Connector (J12)

The MCIMX53SMD board supports a 5 Megapixels CMOS Camera. The CMOS module is based on the OmniVision chipset, OV5642. Auto Focus (AF) function is not supported on the board. The developer can choose another CMOS module on their project, if the pin map is compatible. The MCIMX53SMD board uses CMOS connector, FX12B-40P-0.4SV, from HIROSE.

3.17. Debug UART Connector (on Debug Board)

UART1 of the i.MX53 processor is connected to an RS-232 output to be used as a debug output for the developer. The Transmit (TX) and Receive (RX) signals are sent through two 1.8V to 3.2V level shifters to convert the logic signal voltages to the correct values for the Sipex SP3232 RS-232 transceiver. The CTS and RTS signals are not used on the MCIMX53SMD board. The RS-232 transceiver receives its power from the external 3.3V LDO regulator. If the output of the regulator is turned off for power savings measures, debug output will be lost.

If the designer wishes to use the port as an Applications UART Port, changes can be made in software to reconfigure the port. A male-to-male gender changer can be used to properly convert the port.

To access the debug data output during development, connect the Debug UART Connector to a suitable host computer and open a terminal emulation program (that is, Teraterm or HyperTerminal). Proper settings for the terminal program are:

- BAUD RATE: 115,200
- DATA: 8 bit
- PARITY: None
- STOP BIT: 1-bit
- FLOW CONTROL: None

3.18. JTAG Connector (on the Debug board)

A standard 20-pin ARM JTAG connector is provided on the MCIMX53SMD board. Logic signals to the JTAG connector are 1.8V signals. A 1.8V reference signal is provided to pin one of the connectors so that the attached JTAG tool can automatically configure the logic signals for the right voltage. If the JTAG tool does not have an automatic logic voltage sense, then, make sure that the tool is configured for 1.8V logic.

JTAG tools that have been specifically tested with the MCIMX53SMD board are:

- CodeWarrior (Freescale)
- JTAG Commander (Macraigor)
- J-Link (Segger/Codesourcery)
- J-Link (IAR)

3.19. Expansion Header (J78)

A 120-pin Expansion Port Header is provided on the MCIMX53SMD board which can be used with many optionally expansion boards available from Freescale, or with custom designed boards made be the developer. The Expansion Port makes the following features of the i.MX53 processor available for being used on a custom built expansion card:

- Two Inter-Integrated Circuits (I2C): I2C1, I2C2
- 24-bit data and display control signals
- Resistive Touch Screen Interface
- Various voltage rails

3.20. Function Buttons

The MCIMX53SMD board provides two user interface buttons, which are discussed below.

3.20.1. POWER Button

In the 'Power Off' state, momentarily pressing the POWER button will begin the PMIC power up cycle. The PMIC supplied voltage rails will come up in the proper sequence to power the i.MX53 processor. When the processor is fully powered, the boot cycle will be initiated.

In the 'Power On' state, momentarily pressing the POWER button will send a signal to a GPIO port for user defined action, but will not initiate a hardware shutdown.

In the 'Power On' state, holding the power button down for more than 5 seconds will result in the PMIC initiating a shutdown to the 'Standby' power condition. This will also be the result from the 'Power Off' state as the PMIC will transition into the 'Power On' state and will still see the POWER button as held down.

3.20.2. RESET Button

Pressing the RESET button in the 'Power On' state will force the i.MX53 processor to immediately turn off, and reinitiate a boot cycle from the Processor Power Off state. The RESET button has no effect on the PMIC or the voltage rails.
Pressing the RESET button when the MCIMX53SMD board is powered off will have no effect.

3.21. User Interface LED Indicators

There are eight LED status indicators located next to the micro SD card connector. These LEDs have the following functions:

- 15V: The 15V status LED (D29) is a Red LED connected directly to the 15V power rail. This LED indicates that 15V wall power is being properly supplied to the MCIMX53SMD board.
- CMOS Run/Charger Now: This status LED (D27) is a Red LED gated by the EIM_D30 (W4) GPIO pin with two functions. One of these functions is for CMOS running status, the other is dedicated to the status of charger.
- USER Debug/Charger Done: This LED (D32) is a Green LED gated by the PATA_DATA1 (L3) GPIO pin with two functions. One of these functions is for User debug, the other is dedicated to the status of charger.
- 3G Status: The 3G modem status LED (D19) is an Orange LED gated 3G WWLAN pin.
- WiFi/BT: The WiFi/Bt status LED (D9, D10). D9 is a Green LED, and as WLAN Active status. D10 is a Blue LED, and as BT Active status.

3.22. Li-ION Battery Connector (J12)

The MCIMX53SMD board provides a footprint (J12) that can be used to solder a five-pin connector. The board has a three-cell Li-ION battery of ~40 Wh. The developer can change it, if needed, and must follow the pin map of the connector.

3.23. Back-Up Coin Cell Posts (BT1)

For proper operation, the coin cell posts should be soldered direction to the MCIMX53SMD board. The DA9053 PMIC will charge the coin cell when Battery or Wall Power is available. When Battery or Wall Power is removed, the coin cell will provide power only to the RTC power rail (VLDO1), supplying power to the i.MX53 processor. The length of time a coin cell can power the RTC subsystem may vary.

4. MCIMX53SMD Board Connectors

The MCIMX53SMD board provides a number of connectors for a variety of inputs and outputs to and from the board. The following subsections describe these connections in detail.

4.1. Wall 15V Power Jack (J35)

The 15V at 3A AC-to-DC power supply that comes with the MCIMX53SMD board is plugged into the Power Jack (J35) on the board, as shown in **Figure 4-1**. To avoid damage to the board, it is recommended not to use unofficial power.

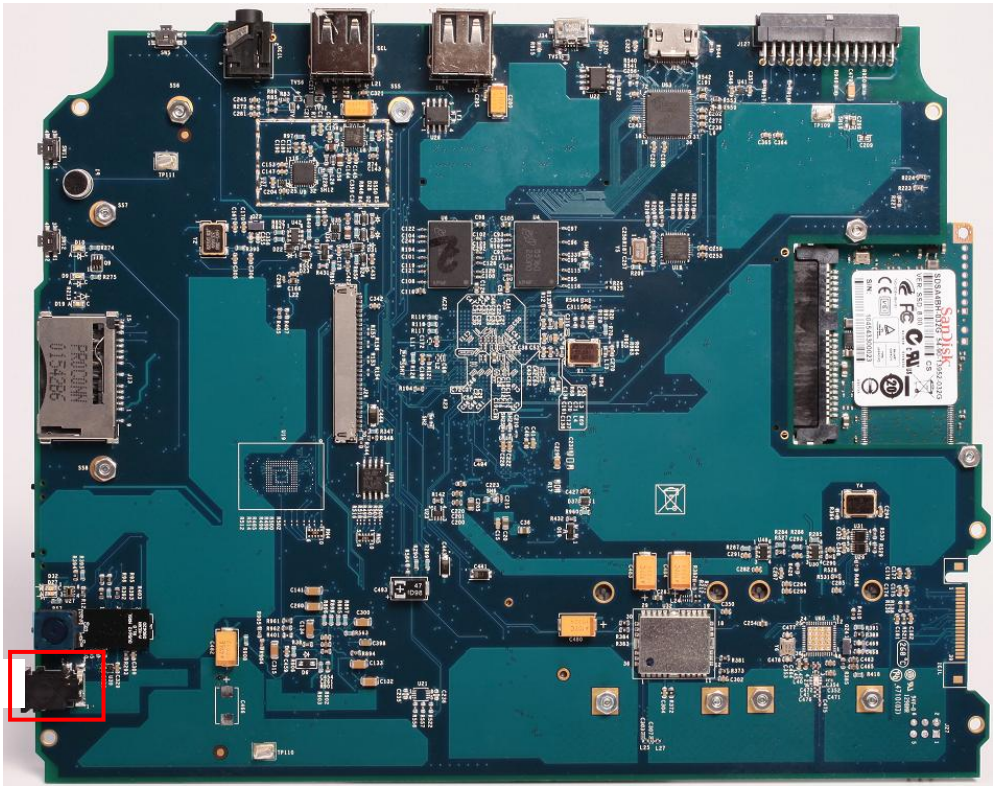


Figure 4-1. DC Power Jack

4.2. SD Card Connector (J13)

The MCIMX53SMD board has one 4-bit SD/MMC connector that can be used for memory, or for third-party SDIO type cards, such as WiFi or Bluetooth. The SD Card Connector (J13) connects a 4-bit parallel data bus to the SD1 port of the i.MX53 processor. The SD Card Connector receives power from DCDC_3V3. The board can be modified to support booting from this connector. See the Boot Mode Operations and Selections section to learn how to modify the board. The SD Card Connector is not spring loaded, so pushing the card into the slot will not initiate an action to disengage the SD Card. The SD Card is inserted facing up at the location shown in **Figure 4-2**.

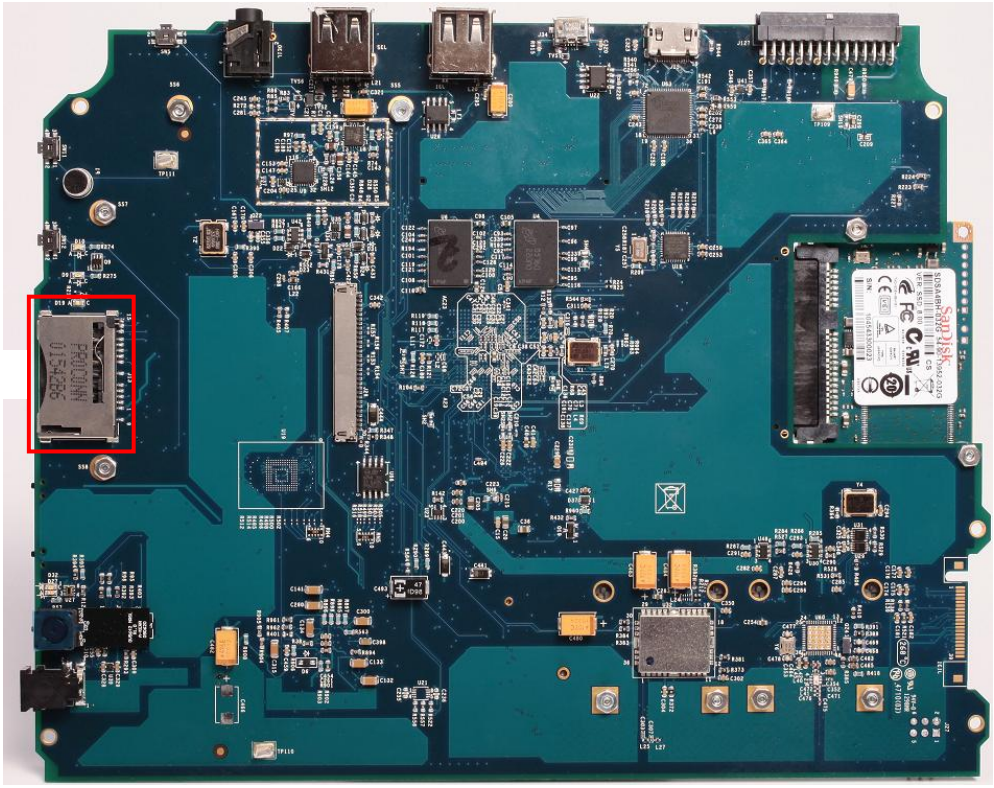


Figure 4-2. SD Connector

4.3. Headphone Output Connector (J130)

Any set of ear buds or headphones with a standard 3.5 mm stereo jack can be connected to the Audio Output jack at the point shown in **Figure 4-3**. Ear buds are not supplied with the MCIMX53SMD board kit.

Headphone Connector (J130)

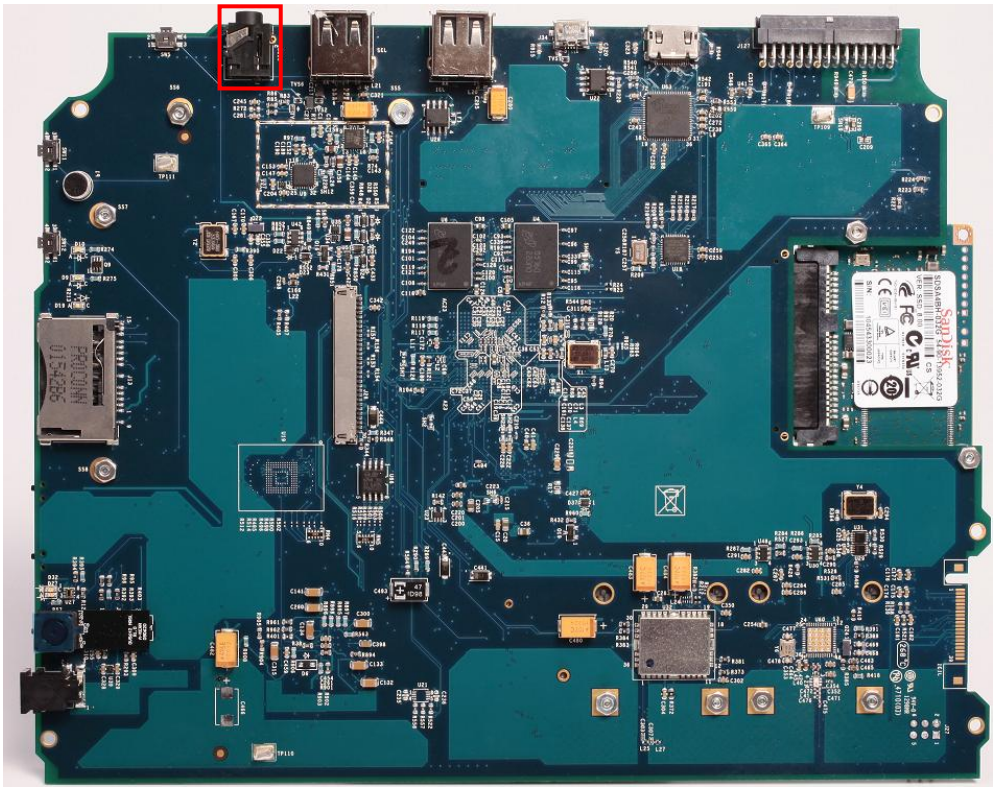


Figure 4-3. Headphone Connector

4.4. Dual USB Host Jack (J31, J32)

The MCIMX53SMD board has two USB Host only connectors that can be used to support USB devices:

- Any single, high-power USB device,
- Any combination of USB devices though a self-powered hub not to exceed 500 mA current draw, or
- Any combination of USB devices through a powered hub.

Dual USB connectors are shown in **Figure 4-4**.

Dual USB HOST Connector (J31, J32)

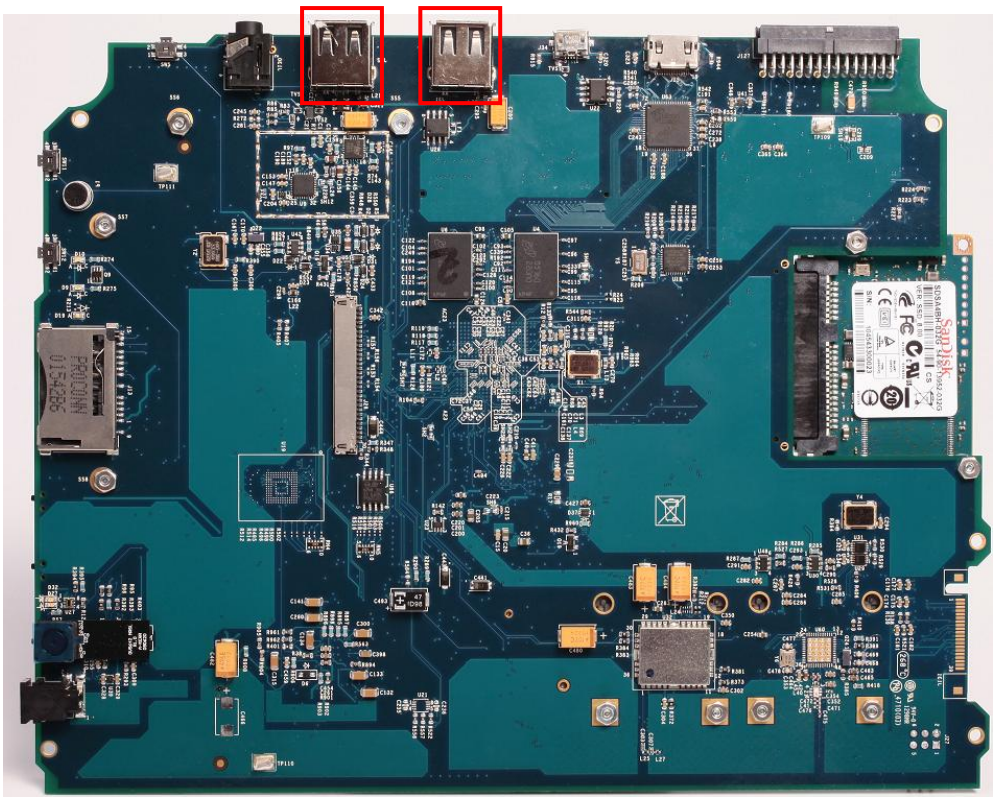


Figure 4-4. Dual USB HOST Connector

4.5. Micro-B USB Device Connector (J34)

The MCIMX53SMD board has one micro-B USB device connector that can be used to connect the MCIMX53SMD board to a USB Host computer. The micro-B connector is connected to the high-speed (HS) USB 2.0 OTG module of the i.MX53 processor. When a 5V supply is provided to the micro-B connector (from the USB Host), then, the i.MX53 processor will configure the OTG module for device mode. This will prevent the lower USB Host port from operating correctly. The 5V power provided by the attached USB Host is only used by the i.MX53 processor for sensing that the host is present. The MCIMX53SMD board will not draw power from the connected USB Host and will not operate without a 5V DC power source or charged Li-ION battery. The micro-B connector is keyed and will not accept a micro-A plug from a cable. A micro-B to USB-A cable is supplied as part of the MCIMX53SMD board kit and can be inserted into the micro-B USB connector at the point shown in **Figure 4-5**.

Micro-B USB Connector (J34)

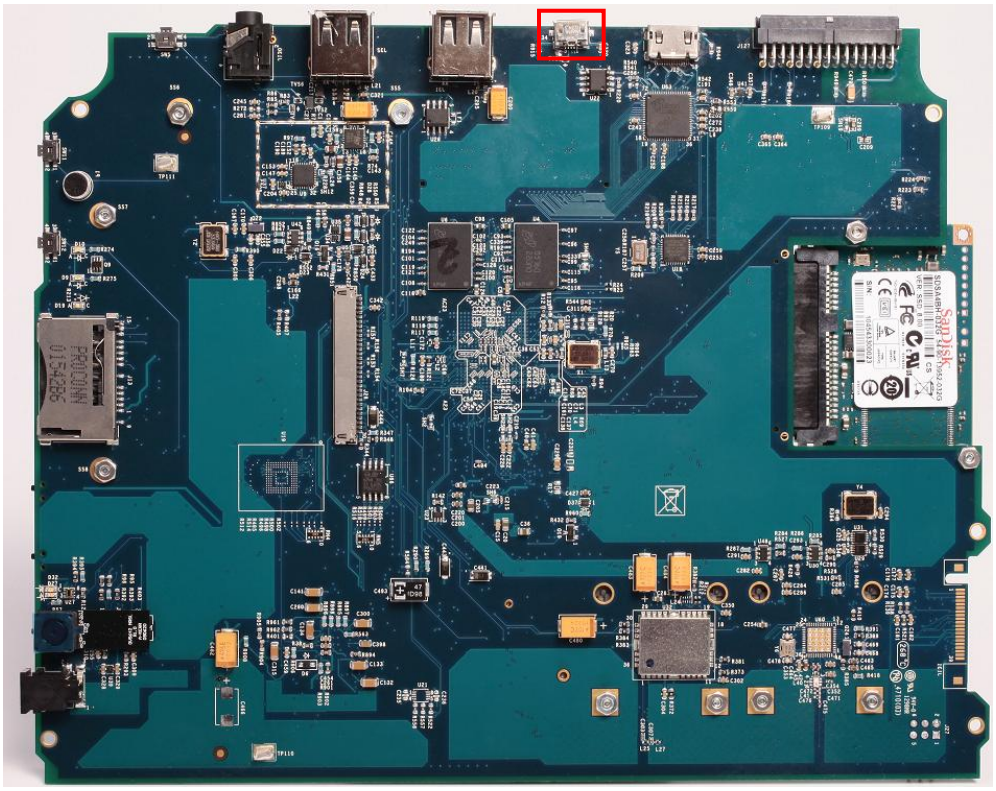


Figure 4-5. Micro-B USB Connector

4.6. Mini-HDMI Connector (J25)

The MCIMX53SMD board has one mini-HDMI connector that can be used to connect the MCIMX53SMD board to HDMI display. The mini-HDMI connector is connected to HDMI transceiver SiI9022. RGB signals and SPDIF are connected with the i.MX53 processor. A mini-HDMI cable is supplied as part of the MCIMX53SMD board kit and can be inserted into the mini-HDMI connector at the point shown in **Figure 4-6**.

Mini-HDMI Connector (J25)

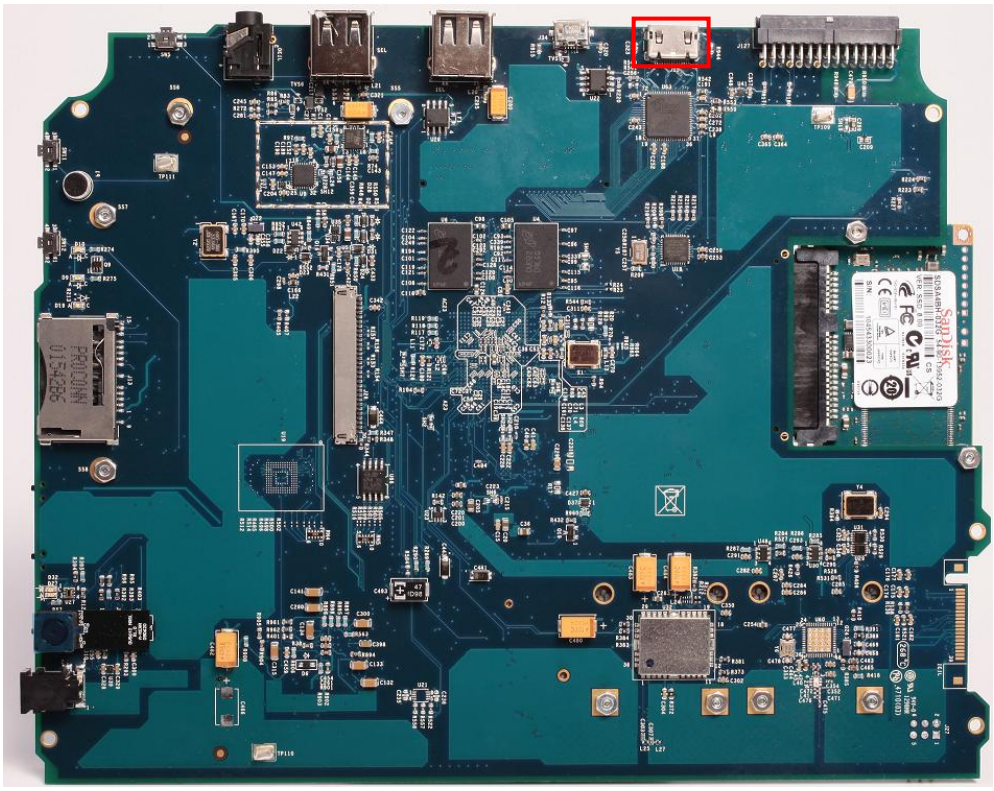


Figure 4-6. Mini-HDMI Connector

4.7. Debug Connector (J127)

The MCIMX53SMD board has one debug connector that can be used to connect the MCIMX53SMD board to the debug board. It includes JTAG, RS-232, and Ethernet. It is easy to use to debug the board for SW engineer. A debug board is supplied as part of the MCIMX53SMD board kit and can be inserted into the debug connector at the point shown in **Figure 4-7**.

A standard Cat-V Ethernet cable is attached to the debug board at the Ethernet. The connector allows the Ethernet IC to auto configure the port for the correct connection to either a switch or directly to a host PC on a peer-to-peer network. It is not necessary to use a crossover cable when connecting directly to another computer. A Cat-V Ethernet cable is supplied as part of the MCIMX53SMD board kit.

To connect a host PC to the MCIMX53SMD board to receive debugging information, a Null Modem serial cable is required and supplied with the MCIMX53SMD board kit. For newer generation computers that do not have a serial port, a USB-to-Serial cable can be used. There is no need for any special cabling to support debug information output.
The debug board contains a standard 20-pin ARM JTAG connector for advanced debugging with a third-party emulator. The header is configured to be used with 1.8V data signals. The developer should exercise caution when selecting the appropriate debugging tools. If an emulator set for 3.3V power and data is connected to the MCIMX53SMD board, the i.MX53 processor will be damaged.

Debug Connector (J127)

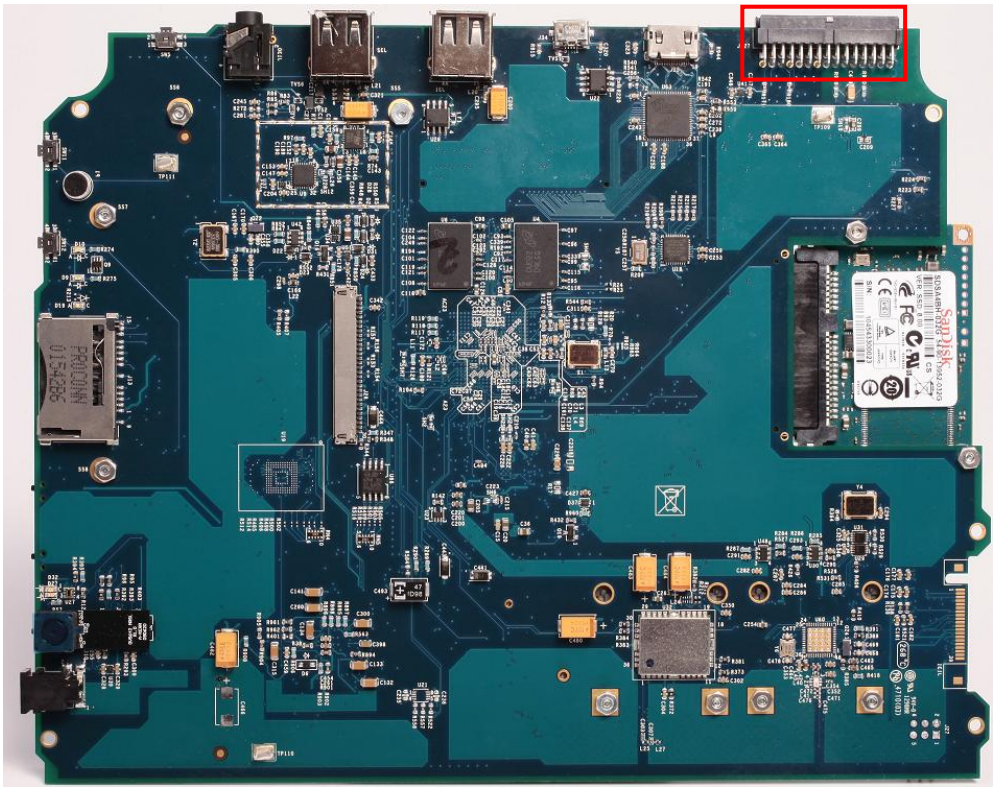


Figure 4-7. Debug Connector

4.8. SATA Connector (J5)

A SATA connector (J15) is provided on the MCIMX53SMD board and is connected to the SATA module of the i.MX53 processor. The MCIMX53SMD board is capable of communicating with any standard SATA device (SSD SATA in the MCIMX53SMD board kit). It is possible to initiate a boot from an attached SATA device. See the software reference manuals for instructions on how to configure the MCIMX53SMD board for SATA boot. The SSD SATA is plugged into the MCIMX53SMD board at the location shown in **Figure 4-8**.

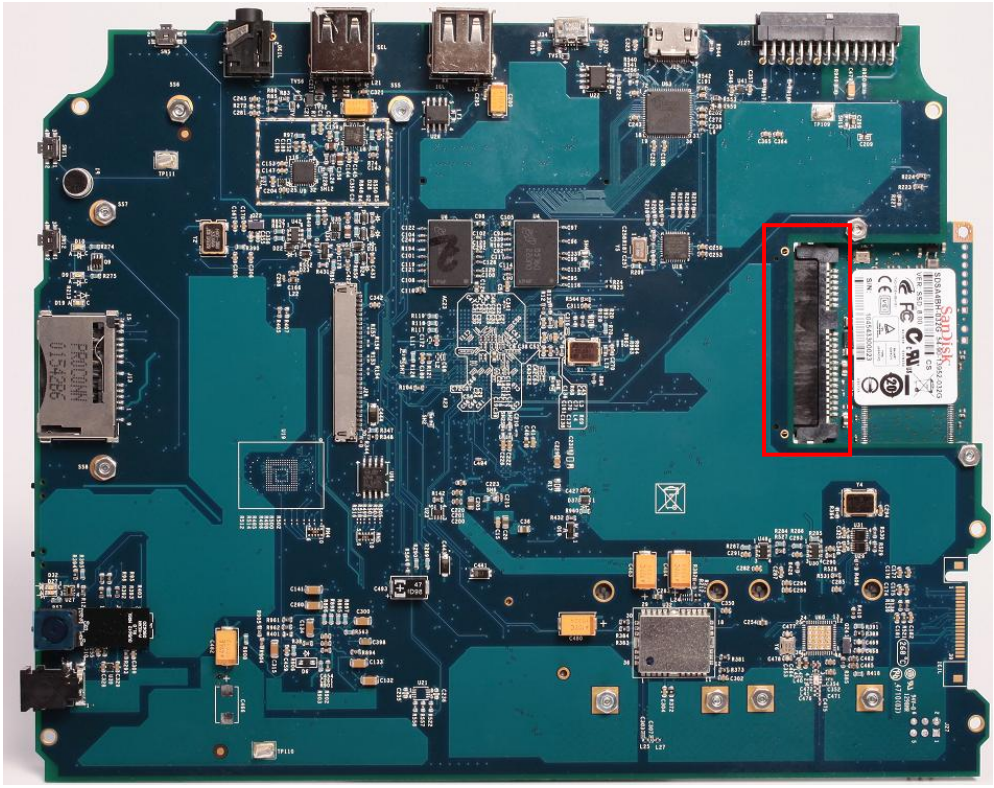


Figure 4-8. SATA Connector

4.9. VGA Dock Connector (J131)

A VGA Dock connector (J131) is provided on the MCIMX53SMD board for future usage. It includes VGA signal, LINE IN/OUT, and USB. The Dock location is shown in **Figure 4-9**.

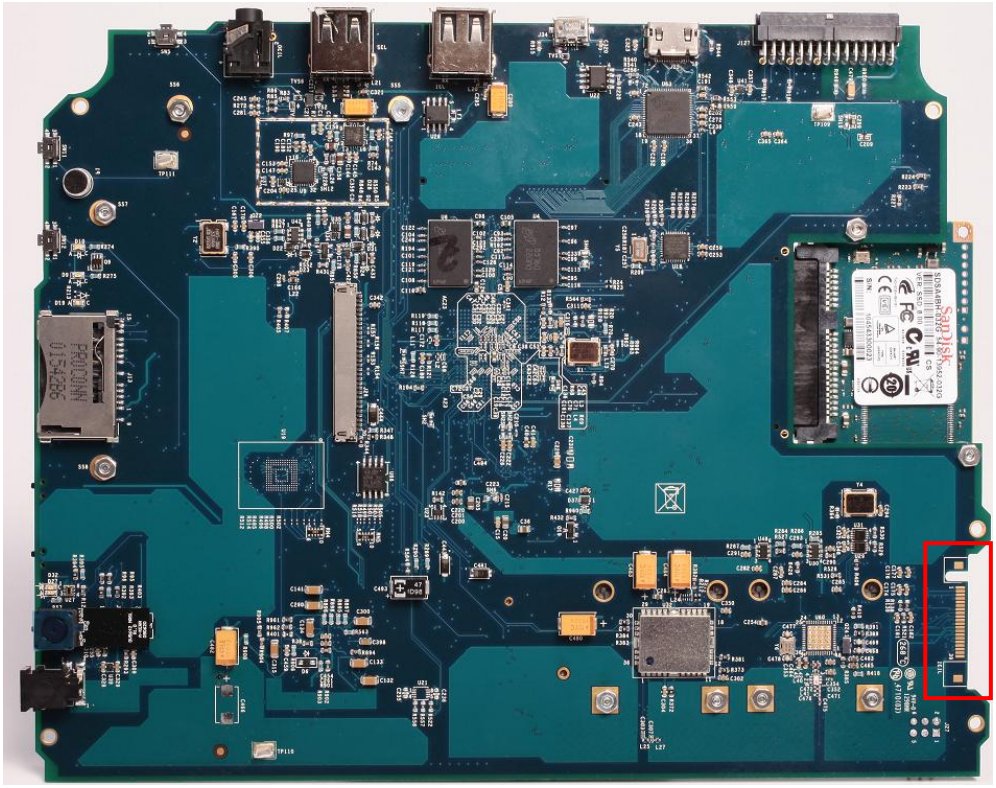


Figure 4-9. VGA Dock Connector

4.10. LVDS Connector (J28, J29)

The MCIMX53SMD board includes two 30-pin (Hirose, DF19G-30P-1H (56)) connectors for using with the LVDS display. Freescale has made available a cable and LVDS1 display (HannStar, HSD100PXN1-A00-C11). The LVDS connectors are located on the top and bottom side of the board in the location shown in **Figure 4-10.**

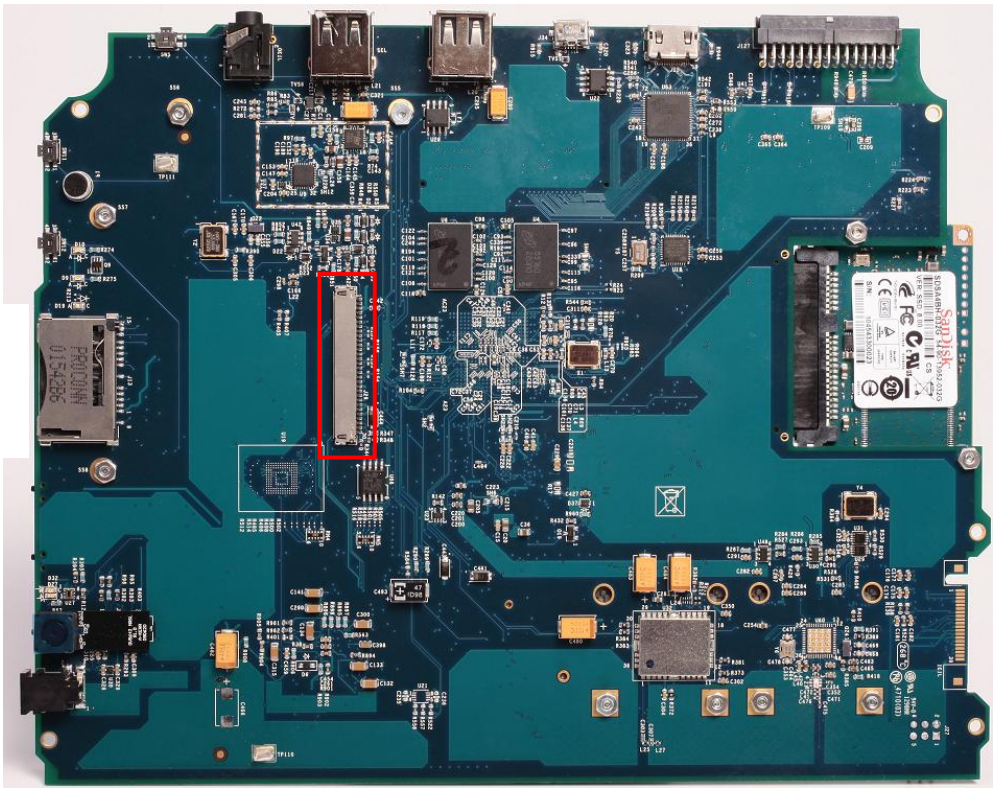


Figure 4-10. LVDS Connector

5. MCIMX53SMD Board Architecture and Design

This section is designed to provide the developer detailed information about the electrical design and practical considerations that went into the MCIMX53SMD board. This section is organized to discuss each block in the high level block diagram of the MCIMX53SMD board shown in **Figure 5-1**.

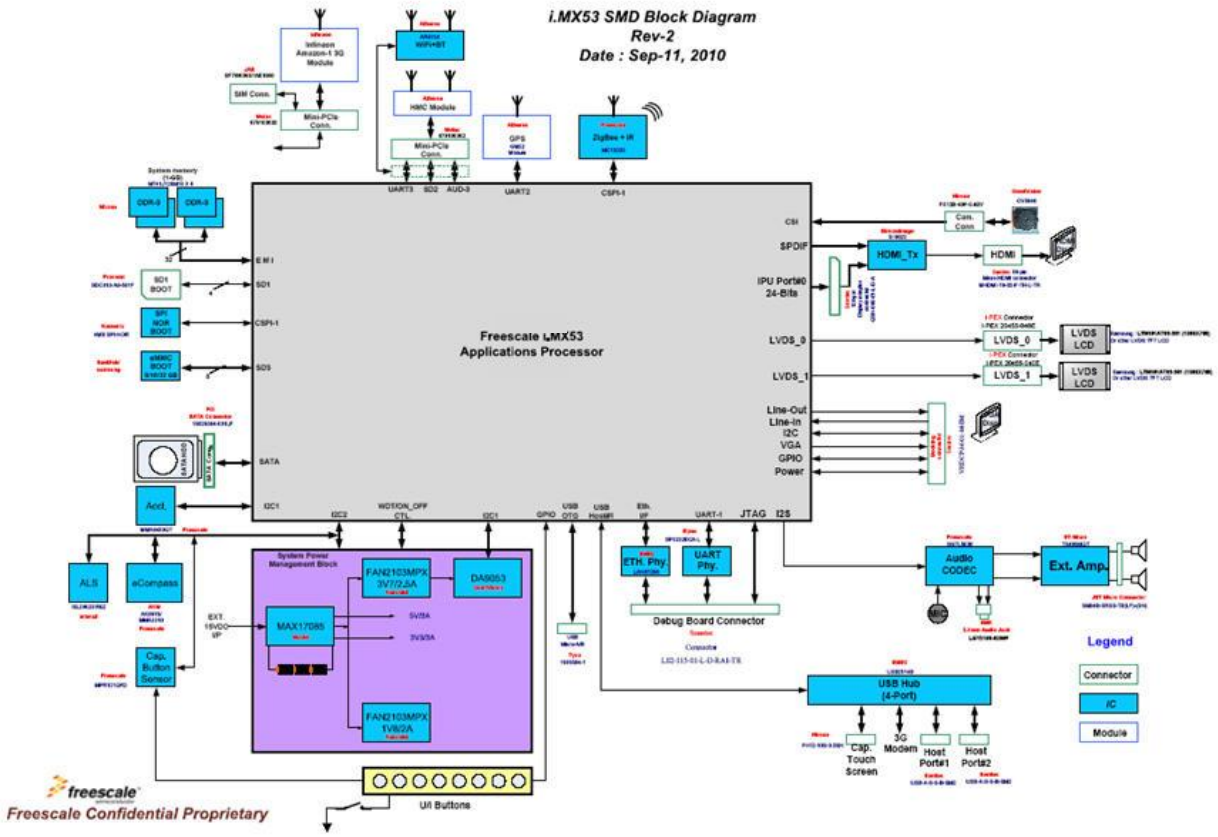


Figure 5-1. MCIMX53SMD Board Block Diagram

5.1. Dual LDO, DCDC, and Charger

The MCIMX53SMD board uses the MAX17085B chip as main power chip. The MAX17085B chip provides two LDOs (3.3V and 5V), two DCDCs (3.3V and 5V), and a multi-cell Li-Ion charger. The MCIMX53SMD board provides a three-cell Li-Ion battery as main power source. A 15V power from an external wall power supply is connected to the MCIMX53SMD board at connector J35. The 15V supply is provided from the connector to the MAX 17085B chip through the current protection fuse (F2).

The MAX17085B LDOs are always turned ON, when power is attached. When the ON/OFF key is pressed, the high signal makes the MAX17085B chip to output two DCDCs (3.3V and 5V), and then power ON the PMIC. The MAX17085B DCDCs have enough current and they are the main source of power for the whole system.

The MAX17085B chip also has charger function. When wall adapter is plugged in, 2A max charge current is fed to the battery.

5.2. Dialog DA9053 PMIC

The Dialog PMIC provides all regulated power to the i.MX53 processor. The PMIC is located in the middle of the MCIMX53SMD board (near to the MAX17085B chip and i.MX53 processor). From this location, power is supplied to the rest of the board.

When the POWER button is pressed for the first time, the MAX17085B chip outputs DCDC_3V3 and DCDC_5V, and feeds to the PMIC. PMIC senses the Active Low signal on the nONKEY pin by RC delay circuit and begins to power ON all voltage rails in preprogrammed sequence. The sequence is determined primarily by the order in

which power must be supplied to the i.MX53 processor. Once the core operations of the processor are fully powered, other power rails can be turned ON.

The first voltage regulator to power ON is always VLDO1. This regulator supplies a maximum of 40 mA current at 1.3V and powers ON only the Secure RTC module of the i.MX53 processor. This turns ON the RTC Clock (32.768 kHz) and Watch Dog features. If a system reset is triggered, or the MCIMX53SMD board is placed into the standby mode, VLDO1 will remain powered ON. VLDO1 will turn OFF only if all power is removed from the MCIMX53SMD board, or if a software command is sent to the PMIC to turn OFF VLDO1. In case, the developer attaches an optional coin cell (BT1), the coin cell will provide the necessary power to keep VLDO1 operating.

The power sequence requirements for the i.MX53 processor (as specified in the i.MX53 data sheet) are as follows:

1. NVCC_SRTC_POW (VLDO1)
2. VCC, VDDA, VDDGP (in any order)
3. NVCC_CKIH, VDD_REG (in any order)
4. All other supplies (in any order)

NOTE

In case the internal regulator is used for VDDA generation, the VDD_REG should be powered up together with VCC and VDDGP, before other supplies. If the internal regulator is not used to generate VDDA (as on the MCIMX53SMD board), the VDD_REG is independent and has no power-up restrictions.

The power up timing sequence shown in **Table 5-1** is the sequence programmed into the Dialog PMIC. It is one way of providing power sequences to the i.MX53 processor. Designers are free to change the power timing sequence on their own board designs as long as the timing requirements are met. Freescale has not formally tested other power up timing sequences.

Regulator	Time Slot
VBUCKPRO	19 mSEC
VBUCKPERI VLDO6 VLDO8 VLDO10	23 mSEC
VBUCKCORE	27 mSEC
VBUCKMEM VBUCKPERI/SW VLDO2 VLDO5	31 mSEC
VLDO4 VLDO7	35 mSEC
VLDO3 VLDO9	64 mSEC

Table 5-1. Regulator Timing Sequence

The Dialog PMIC enters a SHUTDOWN/STANDBY condition in three ways:

- By a command from the i.MX53 processor through I2C communications
- By i.MX53 processor action to hold the nONKEY/KEEPACT pin low for at least five seconds
- By hardware if the user holds down the POWER button for more than five seconds

All three actions result in the Dialog PMIC powering down the voltage regulators in reverse order of the power up sequence, except for VLDO1. Subsequently, pressing the POWER button will initiate the same power up sequence as shown in **Table 5-1**.

The various power rails supplied by the PMIC are discussed in the SMD Power Rails subsection. Other features of the Dialog PMIC implemented by the MCIMX53SMD board are discussed in the Backlight LED Driver, Touch-Screen Operation, and Miscellaneous sub-sections.

5.2.1. SMD Power Rails

Table 5-2 shows all the voltage supply rails used on the MCIMX53SMD board, their voltages and the major subsystems they supply on the board.

Regulator	Voltage	Named Rails	Powers
VBUCKCORE	1.1V	VBUCKCORE VDDGP	VDDGP
VBUCKPRO	1.3V	VBUCKPRO VCC_1V3	VCC
VBUCKMEM	1.5V	VBUCKMEM DDR_1.5V DDRQ_1.5V	NVCC_EMI_DRAM DDR3 SDRAM
VBUCKMEM/SW	1.5V	VMEM_SW DDR_1.5V (ALT) DDRQ_1.5V (ALT)	ALTERNATE FOR: DDR3 SDRAM LOGIC DDR3 SDRAM CORE
VBUCKPERI	2.5V	VBUCKPERI VDD_REG_2V5 NVCC_XTAL_2V5 LVDS_2V5 (ALT) SATA_PHY_2V5 (ALT) VUSB_2V5 (ALT)	VDD_REG NVCC_XTAL ALTERNATE FOR: LVDS MODULE SATA MODULE USB MODULE 2.5V
VBUCKPERI/SW	2.5V	VPERI_SW LVDS_2V5 SATA_PHY_2V5 VUSB_2V5	LVDS MODULE SATA MODULE USB MODULE 2.5V
BOOST	Current Source	VLCD_BLT	EXPANSION PORT
VLDO1	1.3V	VLDO1_1V3_RTC NVCC_SRTC	NVCC_SRTC
VLDO2	1.3V	DIG_PLL_1V3	ALTERNATE FOR: DIG_PLL GPS
VLDO3	3.3V	VLDO3_3V3 SD1_3V3	Debug I2C1/I2C2 BOOT_SEL NVCC-EIM-MAIN NVCC_EIM_SEC NVCC_SD1&2 NVCC_PATA NVCC_FEC NVCC_GPIO NVCC_KEYPAD
VLDO4	2.775V	VIOHI_2V775 LCD_3V2 (ALT)	NVCC_LCD1 NVCC_LCD2 EXPANSION PORT (LCD)

VLDO5	1.3V	VLDO5_1V3 SATA_1V3	SATA MODULE 1.3V
VLDO6	1.3V	VLDO6_1V3 VDDAL_1V3	VDDAL
VLDO7	2.75V	VLDO7_2V75 TVDAC_2V75	VGA MODULE (TV DCA) CMOS Camera
VLDO8	1.8V	VLDO8_1V8	NVCC_RESET NVCC_JTAG NVCC_CKIH NVCC_NANDF NVCC_CSI VDD_ANA_PLL BOOT_SEL Accelerometer De bug
VLDO9	1.5V	VLDO9_1V5	CMOS Camera
VLDO10	1.3V	VLDO10_1V3 VDDA_1V3	VDDAL
DCDC_3V3	3.3V	DCDC_3V3_BB SATA_3V3 FEC_3V3 3V3_WiFi	ETHERNET AUDIO VGA_IO_SIGNALS USB 3.3V SD CARD (SD1) eMMC EXPANSION PORT SATA LVDS0&1 VGA Dock HDMI KEY PAD GPS ZigBee 3G Modem eCompass Light Sensor TPM Accelerometer Debug WiFi
DCDC_5V	5V	DCDC_5V DCDC_5V_BB V_SPKR	SATA AUDIO LVDS0&1 VGA Dock HDMI EXPANSION PORT Debug KEY PAD
DCDC_1V8	1.8V	DCDC_1V8	VGA Dock

		1V8_WiFi	EXPANSION PORT CMOS Camera WiFi
DCDC_15V	15V	DCDC_15V	VGA Dock

Table 5-2. MCIMX53SMD Board Power Supply Rails

5.2.2. Backlight LED Driver

The Dialog PMIC provides a Boost circuit that controls an external MOSFET Q8. The PMIC is capable of driving three independent strings of up to five white LEDs, each with approximately 24V and maximum of 50 mA. The MCIMX53SMD board does not have a direct connection for white backlight LEDs; however, it supplies a connection to the Expansion Port that can be used to support an attached LCD Daughter Card. The Expansion Port uses the LED1_IN, LED2_IN, and LED3_IN ports of the PMIC.

When designing a circuit to use the Backlight LED driver, it is important to connect the cathode (negative) end of the LED string directly to the LED_IN port of the PMIC. The PMIC controls the supply voltage to the Backlight LEDs by ensuring that the voltage sensed on the LED_IN port is above a threshold voltage of 0.7V. If more than one LED_IN ports are used, the lowest port must be above the threshold value. If the designer connects the cathode end of the Backlight LED string to GROUND, the boost circuit will not work.

The MOSFET used in the boost circuit should have a low ON resistance value for best efficiency. The MOSTFET chosen for the MCIMX53SMD board, on semiconductor NTLJF4156NT1G, also contains a necessary diode used in the boost circuitry. This helps reduce the number of components.

5.2.3. Touch-Screen Operation

The Dialog PMIC contains an autonomous Touch Screen Interface that measures the XY positions from a standard four-WIRE resistive touch panel. An analog-to-digital converter (ADC) channel will detect the presence of a pen touch on the panel, and that will trigger a series of voltage measurements on each of the four touch panel wires (X+, X-, Y+, and Y-) by the ADC in a pre-selected sequence. The resulting voltage readings are then reported to the i.MX53 processor for conversion to a panel X-Y position through the I2C communications link.

To ensure the Touch Screen Interface wakes up autonomously with a pen stroke, it is necessary to supply a 1.8V reference voltage to the TSIREF_GPIO_7 pin of the PMIC. It is recommended that one of the high PSSR Regulators of the PMIC be used to supply this voltage. VLDO6 – VLDO9 are possible sources for supplying this reference voltage.

5.2.4. Miscellaneous

It will automatically charge using the programmed charging settings whenever wall power is supplied to the MCIMX53SMD board. When the battery voltage reaches the programmed level, charging will stop. Battery discharge will not begin until wall power is removed from the board and, if a Li-ION battery is attached, the main battery discharges to the battery cut off level.

There are two port ID traces connected from the Expansion Port header to two of the ADC pins of the PMIC. Each unique Daughter Card designed by Freescale has a different resistor value attached to the two ID traces on the Daughter Card. It is possible to use this voltage divider identification system to determine at boot time if a daughter card is attached, and if so, which specific daughter card it is.

Over-Voltage protection is sensed by the DCIN (B4) pin of the PMIC. The voltage sensed by this pin must be between 4.5V and 5.5V. If the voltage meets this threshold value, the voltage seen at DCIN is blocked from the

DCIN_SEL (B3) pin and the P-Channel MOSFET turns ON. Otherwise, DCIN_SEL remains high and power is blocked from the rest of the MCIMX53SMD board.

The TP (L5) pin of the PMIC must be connected to ground. When designing with a 0.5 mm pitch uBGA package, there is limited space for vias and traces under the BGA. To assist with layout, Freescale has confirmed that all pins labeled 'NO CONNECT' on the PMIC are no manner bonded out to the silicon. Therefore, for routing purposes, it is possible to route the trace from an interior pin through one or more 'NO CONNECT' pins, or to place a via directly under a 'NO CONNECT' pin without requiring a via-in-pad technique. If the CAD Layout Engineer decides to place a via under a 'NO CONNECT' pin, the via should not be tented as trapped gases during the assembly process, as this may cause the solder ball from the 'NO CONNECT' pin to blow out into other pins and cause internal shorts under the BGA.

The I2C communications channel between the processor and the PMIC is channel 1. This channel is only shared with the accelerometer. This channel operates at TTL logic level of 1.8V. The NRESET (F10) pin of the PMIC is directly connected to the Active Low POR_B (C19) pin of the i.MX processor. The PMIC will hold the processor in the RESET state until all the power rails are fully powered. The NIRQ (E10) pin of the PMIC is connected to the GPIO_ 16 (C6) pin of the processor. This pin is not a dedicated pin for an interrupt request, but can be programmed in the software to inform the processor that the PMIC has information to be sent to the processor.

The PMIC has several different options for Pull-Up levels on each of its output pins. In some cases, VDD_{OUT} is one option, along with power supplied to both the VDD_IO1 (L4) and VDD_IO2 (K4) pins as Pull-Up source. The exact source of Pull-Up power is determined by the registry settings of the PMIC and can be pre-programmed at the factory as the designer wishes. Some Pull-Up registry settings apply to groups of pins, so care must be taken in selecting the power source for a particular group of pins. See the Dialog PMIC data sheet for more detailed information on registry settings. For the MCIMX53SMD board, VLDO3 (3.3V) is connected to VDD_IO1 primarily to ensure that the 3V3_EN signal sent to the external regulator is sufficient to turn ON the regulator. Similarly, VLDO8 (1.8V) is connected to VDD_IO2 to provide proper I2C TTL logic levels.

5.3. i.MX53 Applications Processor

The i.MX53 Applications Processor is physically located in the central portion of the MCIMX53SMD board. The most critical components for placement after the processor are the DDR3 SDRAM ICs. The remaining components and connectors are arranged around the periphery of the board in locations that minimize trace routing. The i.MX53 processor is a highly integrated system-on-chips with many modules controlled by the main ARM Cortex-A8 core. Most modules have Logic Voltage inputs that allow the designer to modify logic levels to suit the needs of connected ICs. A more detailed explanation of these Logic Voltage Inputs is presented in the Peripheral Module Logic Voltage Levels subsection. The information for voltage levels and other chip specific details come from the i.MX53 data sheet, which is updated time to time.

The i.MX53 processor initializes out of reset according to its preprogrammed ROM code. After initial wakeup, it attempts to read the logic levels on 26 different pins. Depending on which pins are high/low, the processor selects one of the allowed boot options to begin the boot process. This is further explained in the Boot Mode Operations and Selections subsection.
The clock signals required by the i.MX53 processor and the rest of the MCIMX53SMD board are further explained in the Clock Signals subsection. The i.MX53 processor has the ability to supply a limited amount of filtered power for internal purposes using an internal voltage regulator. The operation of this regulator is explained further in the i.MX53 Internal Regulator subsection. The Processor also has an internal Watch Dog Timer (WDOG) circuit that can be used to reset the Processor in the event it stops functioning correctly. The supported circuitry is explained further in the Watch Dog Time subsection.

5.3.1 Peripheral Module Logic Voltage Levels

By convention, pins used on the i.MX53 processor to set module logic voltage levels begin with NVCC_*. This information about i.MX53 processor is important for developers when they are developing projects based on i.MX53 processor. There are 25 such pins, and practically speaking, they supply the internal pull-up voltages for pins designated for data output. These 25 pins are explained in **Table 5-3**. Once a voltage level is selected for a particular module, all pins within that module will use the same voltage level. It is important for the developer not to try to use an external pull-up to a different voltage level for individual pins. Level shifters must be used if certain pins need to have different voltage levels to interface with external ICs. If a different voltage level is used on an external pull-up, one or both of the affected power rails will most likely have a different voltage level than intended, throughout the design. On a newly designed board that shows unexpected voltage levels, this may be the first thing to check.

Pin Name	Module	Allowed Values	MCIMX53SMD board
NVCC_EMI_DRAM_1 NVCC_EMI_DRAM_2 NVCC_EMI_DRAM_3 NVCC_EMI_DRAM_4 NVCC_EMI_DRAM_5	External Memory Interface	1.425V - 1.9V	1.5V (Match DDR3 Memory)
NVCC_NANDF	NAND Flash	1.65V - 3.6V	1.8V
NVCC_EIM_MAIN_1 NVCC_EIM_MAIN_2 NVCC_EIM_SEC	External Interface Module	1.65V - 3.6V	3.3V
NVCC_RESET	Reset Logic Levels	1.65V - 3.1V	1.8V (Match PMIC)
NVCC_SD1	SD Card Module 1	1.65V - 3.6V	3.3V (Match SD Cards)
NVCC_SD2	SD Card Module 2	1.65V - 3.6V	3.3V
NVCC_PATA	Parallel ATA	1.65V - 3.6V	3.3V
NVCC_LCD_1 NVCC_LCD_2	LCD Module	1.65V - 3.1V	2.775V
NVCC_CSI	Camera Sensor Interface	1.65V - 3.6V	1.8V
NVCC_FEC	Fast Ethernet Controller	1.65V - 3.6V	3.3V (Match Ethernet PHY)
NVCC_GPIO	General Purpose I/O	1.65V - 3.6V	3.3V
NVCC_JTAG	JTAG Module	1.65V - 3.1V	1.8V
NVCC_KEYPAD	Keypad Port	1.65V - 3.6V	3.3V (Match Audio CODEC)
NVCC_CKIH	Clock Amplifier Circuit	1.65V - 1.95V	1.8V
NVCC_XTAL	24MHz Crystal Supply	2.25V - 2.75V	2.5V
NVCC_SRTC_POW	Secure Real Time Clock	1.1V - 1.3V	1.3V
NVCC_LVDS	Low Voltage Differential Signaling	2.375V - 2.625V	2.5V
NVCC_LVDS_BG	LVDS Band Gap	2.375V - 2.625V	2.5V

Table 5-3. Module Voltage Supplies

The MCIMX53SMD board has a number of unpopulated pull-up resistors. This is a result of the initial design being conservative, and the addition of external pull-up resistors to supplement internal i.MX53 pull-up supply voltage. Subsequent MCIMX53SMD board usage has shown these pull-ups to be unnecessary, so they are unpopulated.

5.3.2 Boot Mode Operations and Selections

The i.MX53 processor can be directed to boot from:

- The logic levels on 24 different pins that are designated for boot mode configurations
- Internal eFUSE settings
- A serial downloader (USB/UART)

There are two dedicated BOOT_MODE pins in the i.MX53 processor that specify where the processor should find its boot information. **Table 5-4** shows the settings of BOOT_MODE pins for each of these methods.

Developers should remember that these two pins are tied to the NVCC_RESET modules, and therefore, on the MCIMX53SMD board, they use a 1.8V logic level (unlike the Boot Configuration pins that use a 3.3V logic level). The default boot selection for the MCIMX53SMD board is 00 – Boot from hardware settings. The settings of the BOOT_MODE pins can be changed by using the optional DIP switches, SW28.3 and SW28.4. It is less likely that developers want to boot the processor from eFUSEs as eFUSEs may get damaged during the boot process. Developers can use the serial downloader method to boot the processor by turning both the DIP switches to ON.

BOOT_MODE1	BOOT_MODE0	Boot Selection
0	0	Boot from hardware settings
0	1	Reserved
1	0	Boot from eFUSE settings
1	1	Use serial downloader

Table 5-4. BOOT_MODE Pin Settings

If hardware settings are used to boot the processor, then, i.MX53 pins are sampled at the beginning of the boot process. These pins are explained in **Table 5-5A** and **Table 5-5B**, along with their default setting on the MCIMX53SMD board. Note that three bits in the BOOT_CFG words do not have corresponding pins to read.

The MCIMX53SMD board supports four types of boot sources: SPI NOR, SD Card (eSDHC1), eMMC4.4 (eSDHC3), and SSD SATA. So, we only keep the relative configure pins for the boot source.

	BOOT_ CFG2[5]	BOOT_ CFG2[6]	BOOT_ CFG2[7]	BOOT_ CFG1[3]	BOOT_ CFG1[4]	BOOT_ CFG1[5]	BOOT_ CFG1[6]	
PIN	EIM_DA0	EIM_EB1	EIM_EB0	EIM_A18	EIM_A19	EIM_A20	EIM_A21	
Default	0	0	0	0	0	0	0	
SW26	1	2	3	4	5	6	7	

Table 5-5A. BOOT_CFG Word1

	BOOT_ CFG3[5]	BOOT_ CFG3[4]	BOOT_ CFG3[3]	BOOT_ CFG2[2]				
PIN	EIM_DA6	EIM_DA7	EIM_DA8	EIM_DA9				
Default	0	0	1	1				
SW28	1	2	3	4				

Table 5-5B. BOOT_CFG Word2

The four pins that determine where bootable code is stored are BOOT_CFG1[6:3]. Depending on which boot source is selected, some of these pins may have different meanings. Those pins will show up as an 'X' for logic level. The specific logic levels and their meanings are as follows:

BOOT_CFG1[6:3] Boot Code Source Selection

010X - PATA/SATA Boot

011X - Serial ROM (I2C/SPI) Boot
1XX0 - SD/MMC (eSD/eMMC) Boot

For each of the bootable source selections, the remaining BOOT_CFG pins have different meanings. The pins are meant to choose initialization settings required for each specific boot source. The following paragraphs will specify those choices based on bootable source:

HD (PATA/SATA)

BOOT_CFG1[3]	HD Type	0 – PATA 1 – SATA

Serial-ROM

BOOT_CFG1[3]	Serial ROM Select	0 – I2C 1 – SPI
BOOT_CFG2[5]	SPI Addressing	0 – 2-byte (16-bit) 1 – 3-byte (24-bit)
BOOT_CFG3[5:4]	Port Select	00 – I2C1/eCSPI1 01 – I2C2/eCSPI2 10 – I2C3/CSPI 11 – Reserved
BOOT_CFG3[3:2]	Chip Select (SPI Only)	00 – CS0 01 – CS1 10 – CS2 11 – CS3

SD/eSD

BOOT_CFG1[4]	Fast Boot	0 – Regular 1 – Fast Boot
BOOT_CFG2[5]	Bus Width	0 – 1-bit 1 – 4-bit
BOOT_CFG3[5:4]	Port Select	00 – eSDHC1 01 – eSDHC2 10 – eSDHC3 11 – eSDHC4

MMC/eMMC

BOOT_CFG1[4]	Fast Boot	0 – Regular Boot 1 – Fast Boot
BOOT_CFG2[7:5]	Bus Width	000 – 1-bit 001 – 4-bit 010 – 8-bit 011 – Reserved 100 – Reserved 101 – 4-bit DDR (MMC 4.4) 110 – 8-bit DDR (MMC 4.4) 111 – Reserved
BOOT_CFG3[5:4]	Port Select	00 – eSDHC1 01 – eSDHC2 10 – eSDHC3 (eMMC4.4) 11 – eSDHC4
BOOT_CFG3[3]	DLL Override	0 – Use Default ROM 1 – Use eFUSE DLL Override

When the MCIMX53SMD board was originally designed, several of the BOOT_CFG pins were selectable by the two 8-position DIP Switch (SW26, SW28). After initial testing of the MCIMX53SMD board, the optimum BOOT_CFG settings for flexibility and ease of use were determined. These are the default settings on the board, which set the eMMC4.4 (eSDHC3) as the default boot source. As the developer becomes more familiar with the board and wishes to experiment more, the next step for the developer is to write code for other device to initialize it as alternative boot source and pass the boot process to the new source.

Figures 5-2 shows the location of BOOT Switch. The ON state indicates high (Power) logic level and the OFF state indicates low (GND) logic level.

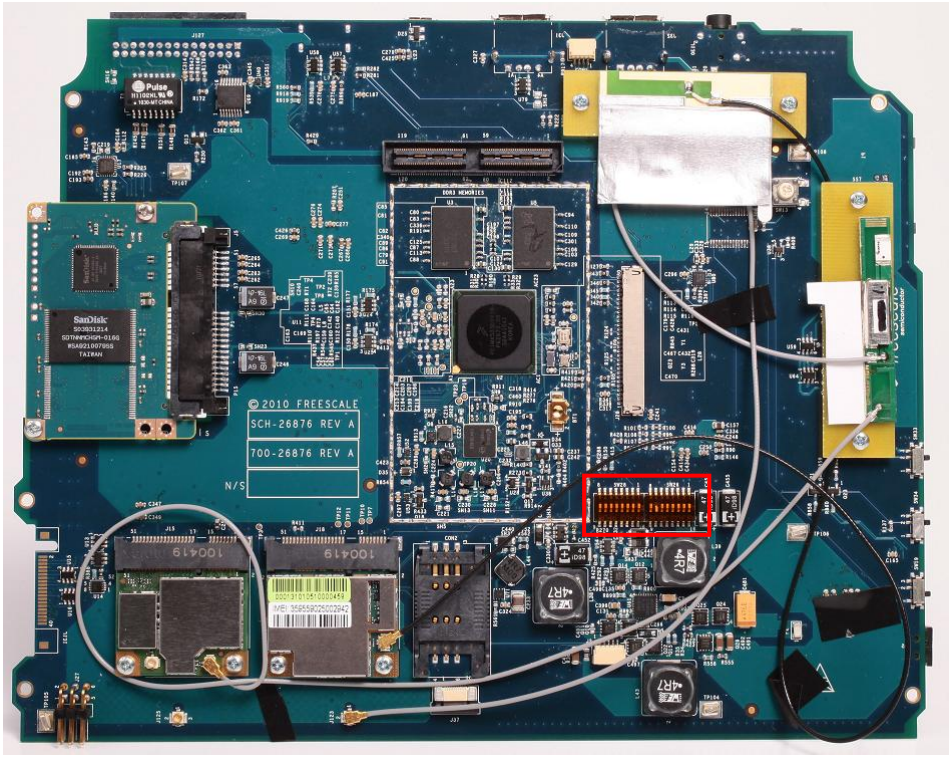


Figure 5-2. Boot Switch (SW26, SW28)

5.3.3 Clock Signals

The i.MX53 processor uses three external clocks: Y1, Y3, and QZ3. The 24 MHz crystal (Y1) is the main clock source for the processor. The crystal is located on the bottom side of the board as shown in **Figure 5-3**. It is driven by its own 2.5V supply pin, NVCC_XTAL. Although the crystal frequency for the board is set to be 24 MHz, the default BOOT_CFG2[2] pin that controls the frequency is left to auto detect. In the case of 24 MHz, the actual setting is not important. If a clock oscillator is used, it would be connected to the pin EXTAL (AB11), and the pin XTAL (AC11) would be left floating. The 24 MHz clock signal can be outputted from any GPIO pin for being used in other locations. On the MCIMX53SMD board, the clock signal is outputted from the GPIO_0 pin and the net is labeled GPIO_0(CLK0). The clock signal is sent to the Audio Codec as the clock source for the audio sub-system, and it is also sent to the expansion port as an available clock signal for a custom designed card, if needed.

The 22.5792MHz OSC(Y3) is the clock source used by the i.MX53 processor and Audio Codec for high performance. It receives power from the VLDO8 1.8V voltage regulator and can be shut by GPIO OSC_CKIH1_EN. The location of the crystal is also shown in **Figure 5-3**.

The 32.768 kHz crystal (QZ3) is the clock source used by the i.MX53 processor for the Secure Real Time Clock module. It receives power from the NVCC_SRTC pin, which is connected to the VLDO1 1.3V voltage regulator. The 32.768 kHz clock signal is not sent anywhere else on the MCIMX53SMD board. The location of the crystal is also shown in **Figure 5-3**.

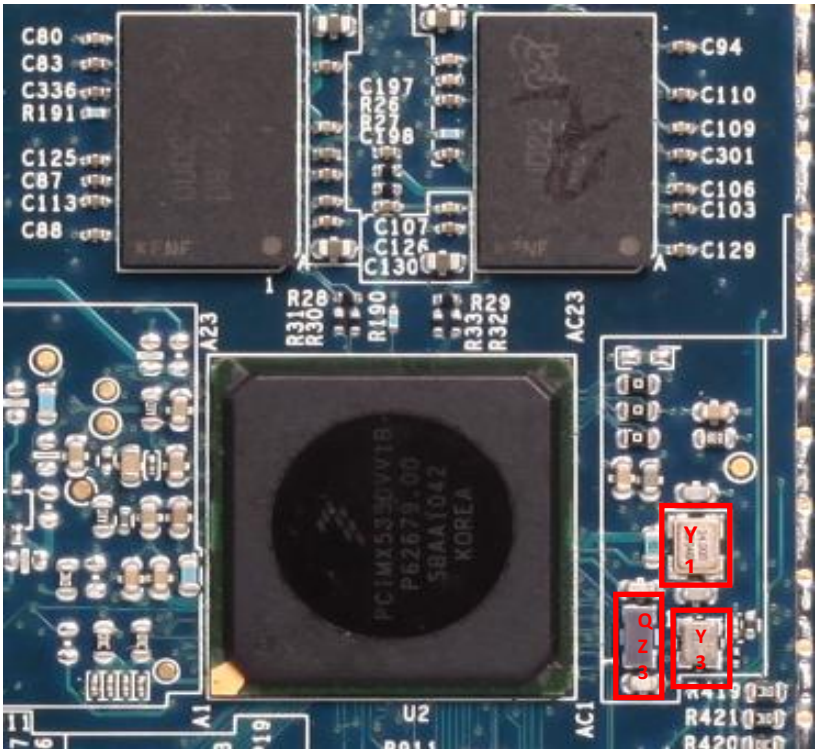


Figure 5-3. Clock Source Locations (Top)

The clock source for the Ethernet PHY is a 50 MHz Oscillator (X1) with an enable pin and is shown in **Figure 5-4**. The oscillator was originally placed to support both the SATA module and the Ethernet PHY. It is no longer used for the SATA module, and only supplies a clock signal to the Ethernet PHY. It is powered by the DCDC_3V3 power rail and, by default, and can be shut by GPIO SATA_CLK_GPEN.

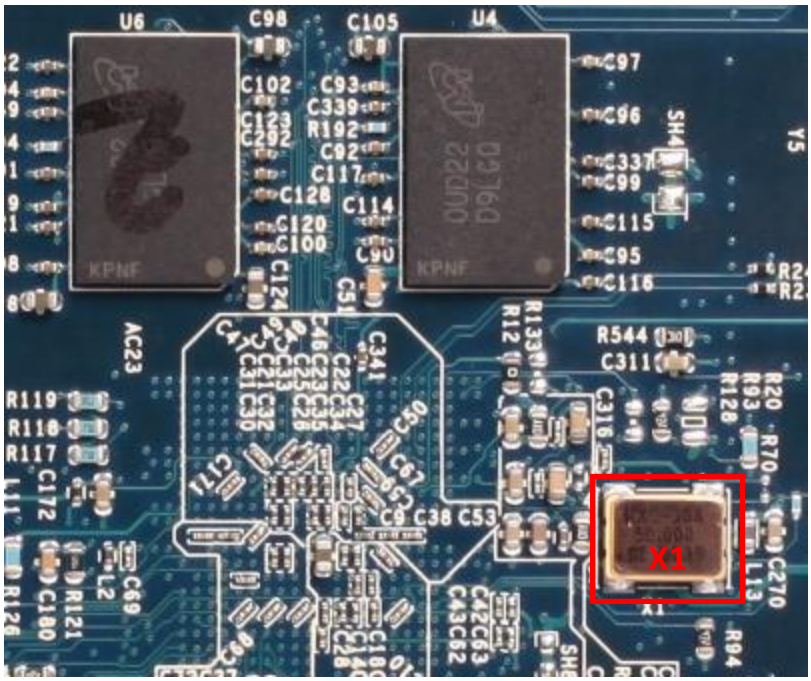


Figure 5-4. Clock Source Locations (Bottom)

5.3.4 i.MX53 Internal Regulators

The i.MX53 Applications Processor contains two internal voltage regulators which can supply VDDA, VDDAL, VDD_DIG_PLL, and VDD_ANA_PLL. The power input for this pin is VDD_REG (pin G18). On the MCIMX53SMD board, this pin is connected to VBUCKPERI and is set to 2.5V.

The Digital PLL voltage regulator can be selected to supply VDD_DIG_PLL through an internal (on die) connection. The VDD_DIG_PLL pin can also be connected to the VDDA and VDDAL pins through an external connection to allow the Digital PLL regulator to supply these rails as well. The Digital PLL regulator is set to start at a reduced voltage value of 1.2V, but is programmed by software to increase to 1.3V in the beginning of the boot process. On the MCIMX53SMD board, the VDD_DIG_PLL connection to VLDO2 is not populated by default, so that VDD_DIG_PLL power is supplied by the internal regulator. The VDDA supply pins are connected to VLDO10 through a shorting trace SH22. If the developer wishes to experiment with supplying VDDA from the internal regulator, the trace between the two pads of SH22 can be cut. The VDDAL supply pin is connected to VLDO6 through a shorting trace SH24. If the developer wishes to experiment with supplying VDDAL from the internal regulator, the trace between the two pads of SH24 can be cut.

The Analog PLL voltage regulator can be selected to supply VDD_ANA_PLL through an internal (on die) connection. The Analog PLL is set to supply a voltage of 1.8V. On the MCIMX53SMD board, the VDD_ANA_PLL connection to VLDO8 is not populated by default, so that VDD_ANA_PLL is supplied by the internal regulator.

NOTE

Developers should note that during the boot process, VDD_DIG_PLL takes ~ 310 ms to change from 1.2V to 1.3V. During this time, the i.MX53 core will not run at full speed/maximum processor loading, rather it will operate in the reduced power mode, with some limitations. The limitations of the reduced power mode are discussed in the i.MX53 data sheet. It is expected that during the first 310 ms, processor loading will not be an issue.

5.3.5 Watch Dog Timer

The i.MX53 processor has an internal Watch Dog Timer circuit. On the MCIMX53SMD board, the WDOG output is assigned to GPIO_9. The WDOG is an active low signal. The Dialog PMIC does not have a specific pin to accept a Watch Dog signal to force a processor reset. Therefore, the WDOG signal is modified by hardware components on the MCIMX53SMD board and applied to the Processor Reset pin (POR_B, pin C19). It allows the processor to reset the WDOG signal and then come out of reset. The buffer IC is also in a tri-state condition when the WDOG signal is normally high, thus allowing the push-button reset circuitry to work. The Watch Dog circuitry is shown in **Figure 5-5**.

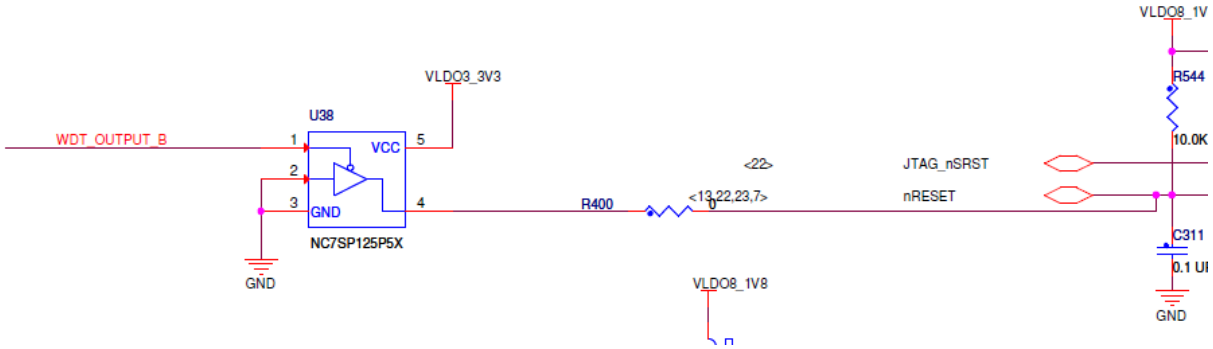


Figure 5-5. Watch Dog Timer Reset Trigger

5.4. DDR3 SDRAM Memory

The MCIMX53SMD board has four 128MX16 DDR3 SDRAM chips for a total of 1 GB RAM memory. The chips are organized in two different arrays, differentiated by the chip selects, storing either the upper 16-bits or the lower 16-bits of a 32-bit word. This organization is shown in **Table 5-6**.

	Chip Select '0'	Chip Select '1'
Lower 16-bits [15:0]	U3	U4
Upper 16-bits [31:16]	U5	U6

Table 5-6. DDR3 SDRAM Chip Organization

In this organization, there are 21 traces that connect to all four DDR3 chips and the i.MX53 processor (14 Address, 3 Bank Address, 3 Control, and Reset). These are the most critical traces since they will see the most loading. The remaining traces are connected to two DDR3 chips and the processor, and will only see one active DDR3 chip at a time. Note that the two clock traces are tied with the data traces (SDCLK_0 for the lower 16-bits, SDCLK_1 for the upper 16-bits). This limits the clock traces to only one active DDR3 chip at a time.

In the physical layout, the DDR3 chips are placed to minimize routing of the address traces. The two chip select '0' chips are placed on top, and the two chip select '1' chips are placed on the bottom side, directly below the chips with the same data traces. The data traces are not necessarily connected to the DDR3 chips in sequential order, but for ease of routing, are connected as best determined by the layout and other critical traces. The i.MX53 processor has the capability of remapping SDRAM word bit order based on chip select used, so that words can be physically stored in memory in correct order. If this is a feature the developer wishes to implement, there is more information in the software reference manual.

The DDR_VREF is created by a simple voltage divider using 470Ω 1% resistors and 0.1 µF capacitors for stability. The relatively small value resistors provide enough current to maintain a steady mid-point voltage. The calibration resistors used by the four DDR3 chips and the processor are 240Ω 1% resistors. This resistor value is specified by the DDR3 specifications. There is a 200Ω resistor between each clock differential pair to

maintain the correct impedance between the two traces. The DDR3 SDRAM should be rated for 1066 MHz or faster.

For skilled designers wishing to double the amount of DDR3 SDRAM available for being used with the i.MX53 processor using eight x8 width DDR3 chips, the following considerations should be weighed carefully before proceeding: Four DDR3 chips on a chip select line will exceed the current supply capability of the VBUCKMEM power source. An additional 1.5V power source would need to be added. Also, attaching the address lines to eight DDR3 chips is a great amount of loading. Premium PCB materials would be required to reduce losses. Using eight DDR3 SDRAM chips in this manner has not been tried by Freescale, and is not formally recommended.

5.5. SD Card Connector

The SD Card Connector (J13) is directly connected to the eSDHC channel 1 module of the i.MX53 processor. This card socket will support up to a 4-bit data transfer from an SD card or a MMC card inserted into the socket. The main power for the SD Card Socket is 3.3V from DCDC_3V3_BB. The developer should note that the internal i.MX53 processor eSDHC module is powered by a 3V3 source. Therefore, changing the voltage of the card socket on the MCIMX53SMD board is not recommended.

The SD1 Clock trace has a 22Ω series termination resistor (R412). This resistor is inserted to prevent a reflected signal from being sensed by the i.M53 processor. This has been found to occur on MMC card operation and is recommended for all designs. In addition, for 50 MHz performance, all SD signals should have equal length.

5.6. eMMC 4.4

One eMMC4.4 is directly connected to the eSDHC channel 3 of the i.MX53 processor. This port will support 8-bit data transfer from eMMC. The main power for the eMMC is 3.3V from DCDC_3V3_BB. The SD3 Clock trace has a 22Ω series termination resistor (R146). This resistor is inserted to prevent a reflected signal from being sensed by the i.M53 processor. This has been found to occur on MMC card operation and is recommended for all designs. In addition, for 50MHz performance, all SD signals should have equal length.

5.7. HDMI

The MCIMX53SMD board has a mini-HDMI that can playback 1080p. The MCIMX53SMD board uses SiI9022 from Silicon Image as HDMI bridge on board. The i.MX53 processor controls SiI9022 through the I2C port. IPU parallel interface and SPDIF are connected with SiI9022.

The SiI9022 HDMI transmitter supports the High Definition Multimedia Interface (HDMI) Specification on a wide range of mobile products. High definition camcorders, digital still cameras, and personal mobile devices connect directly to a large installed base of HDMI TVs and DVI PC monitors, by using the flexible audio and video interfaces provided by this ultra-low-power solution. S/PDIF or I2S inputs enable a pure digital audio connection to virtually any system audio processor or codec. This transmitter is the next generation of its family and is an enhanced replacement for the SiI9022/SiI9022 device, with lower power and enhanced features. The SiI9022 transmitter supports High-bandwidth Digital Content Protection (HDCP) for devices that require secure content delivery.

5.8. VGA Video Output

The TV Encoder module of the i.MX53 processor provides three component video output signals that can be used as either a TV signal or a VGA signal to a connected monitor. The MCIMX53SMD board configures these signals for being used as a VGA output through connector, J131. In addition to the three video signals, Horizontal and Vertical Synchronization signals, I2C Data and Clock, and a 5V reference signal are connected to

the VGA Dock. The video data signals are referenced to 2.75V (TVDAC_2V75), while all other signals are referenced to 5V. The synchronization signals leave the i.MX53 processor referenced to 3.3V, but go through a pair of one-way level shifters (U12, U13) to meet the VGA standard required 5V reference. Similarly, the I2C channel 2 signals leave the processor referenced to 3.3V, but go through a bi-directional level shifter (U14) to also get referenced to 5V. See the VGA Dock Connector (J131) section for actual pin-out of J131 connector.

The Component Video signals are terminated to ground, each with a 75Ω resistor to meet cabling requirements. A separate VGA ground plane has been created to minimize noise on the video signals by necking through a small trace. The voltage reference signal for the TVDAC module is provided by placing a 1.05K 1%Ω resistor at pin Y18. The constant current source provided by the TVDAC module generates the exact voltage reference required by the VGA standard. A 0.1 µF capacitor should be connected to pin AA19 to reduce noise on the voltage reference sense point. Each of the Component Video output traces should be connected to their respective feedback pins. This enables the Cable Detection (CD) circuitry to detect whether or not a cable has been plugged into the connector. The CD circuitry is not active for TV signal output, so it would not be necessary to connect the feedback circuit in that case. If any signal filtering or conditioning components are added to the Component Video traces, the feedback pins should be connected after the additional components (it means, feedback pins should tap into to the connector side of the Component Video signals). It is recommended to use a ferrite bead near the voltage input pins of the TVDAC module in order to reduce noise in the video module.

Besides VGA signal, LINE IN/OUT and USB are included in the VGA Dock. Developers can make their own board for this Dock. The MCIMX53SMD board uses the Dock connector ERF8-020-01-L-D-EM2-TR from SAMTEC. Developers need to choose a suitable connector for their board.

5.9. LVDS Video Output

The i.MX53 processor contains two separate LVDS modules that can be operated independently. Each module provides five sets of differential pair signals: four are used for data signal and one for clock signal. The MCIMX53SMD board uses one of the two modules to provide an optional secondary display panel that can be used in conjunction with one of the other primary means of video output, or as the sole video output, if needed. The MCIMX53SMD board makes use of three of the differential pair data pins and the clock pins. These signals, combined with a display enable pin, a contrast pin, two separate channels of I2C communications, an interrupt pin, and power supplies (5V and 3.3V) will provide the necessary signals to support many of the LVDS display panels currently available in the market. The connector used is a 30-pin connector that meets the LVDS standards for connectors (Hirose, DF19G-30P-1H (56)).

In the MCIMX53SMD board, development work with LVDS panels was done with the Hannstar HSD100PXN1-A00-C11 display. If the developer wishes to use a different LVDS display, a custom cable would most likely be required to ensure that the plug on the cable end, which is connected to the display, was of the right type, and to re-order the signals to match the ordering on the display. For using with other displays, signals are referenced to the following voltages:

- LVDS Data/Clock: 2.5V (LVDS_2V5)
- Display Control: 3.3V (VLDO3_3V3)
- I2C channel 2: 3.3V (VLDO3_3V3)
- I2C channel 3: 3.3V (VLDO3_3V3)

Isolation resistors on the I2C channel 2 traces provide a means of isolating the LVDS connector from other functions on the board, if the LVDS connector is interfering with I2C communication. In addition, the empty pads can also serve as attachment points for hand soldered wires, if the developer wishes to run different signals to this connector.

The i.MX53 processor has an internal method and an external method to measure Band Gap resistance. If the internal method is chosen by the software, pin AA14 can be left floating. If the external method is desired, a 28.0K 1%Ω resistor should be attached between pin AA14 and ground. It is recommended to add this resistor routinely to give software the option of choosing between the two methods. It is also recommended to place a 49.9 1%Ω resistor as the voltage input pin of U14 (NVCC_LVDS_BG) to filter the power used in measuring the Band Gap resistance.

5.10. Expansion Port

The function of the MCIMX53SMD board Expansion Port is to bring out many of the i.MX53 pins that are otherwise unused on the MCIMX53SMD board. The overriding design considerations for this port were to be able to support HDMI functionality through a daughter card (primary), while also being able to support an existing LCD daughter card (secondary). In meeting these considerations, the Expansion Port was also constrained to meet a general power/signal format adopted across all recent i.MX development board designs, primarily for safety and equipment damage consideration. For these reasons, there may be some functionalities of the i.MX53 chip that are not accessible on the MCIMX53SMD board.

For developers who are interested in designing custom daughter cards to be used with the MCIMX53SMD board, the following capabilities are available from the Expansion Port. Note that many pins are muxed, so that not all features are available at the same time:

- Two Serial Peripheral Interfaces (SPI) — CSPI, eCSDPI2
- Two I2S/SSI/AC97 Ports — AUDMUX4, AUDMUX5
- Two Inter-Integrated Circuits (I2C) — I2C1, I2C2
- 2 UARTs — UART4, UART5
- SPDIF Audio
- USB ULPI Port — USBH2
- 24-bit Data and display control signals
- Resistive Touch Screen Interface

In addition to the Data/Signal traces to support the above functionality, the following power sources are also included on the Expansion Port:

• 5V_MAIN	5V	DCDC_5V
• LCD_3V3	3.3V	DCDC_3V3
• VIOHI_2V775	2.775V	VLDO4
• VLDO8_1V8	1.8V	VLDO8
• VLDO9_1V5	1.5V	VLDO9
• VLCD_BLT	Current Source	PMIC LED Driver

Note that VLDO9 is only used by the Expansion Port on the MCIMX53SMD board. The developer is free to reprogram the LDO regulator on the PMIC for desired voltage with these limitations:

- Voltage 1.25V – 3.6V
- Current 100 mA

A suitable connector to be used with Expansion Port J13 is one developed by Samtec, QTH-060-XX-L-D-A, where XX determines the height of the connector. See the Connector Pin-Outs section to know about the available pin-mux options.

5.11. Audio

The main Audio CODEC used on the MCIMX53SMD board is the Freescale SGTL5000 Low Power Stereo Codec with Headphone Amp. The i.MX53 processor provides digital sound information from the AUDMUX module

channel 5 port through I2S communications protocol. The Audio CODEC also receives command instructions from the I2C channel 2 bus and receives a 24 MHz clock input signal from GPIO_0 of the i.MX53 processor. These seven connections with the processor are the only required signals.

The Audio CODEC provides a Left and Right Stereo output signal capable of providing a 16Ω set of headphones/earbuds with up to 58 mW of power. The Audio CODEC is also capable of receiving a single microphone channel, and converting the information to a digital format and transmitting it back to the processor. The CODEC also generates the necessary microphone bias voltage to allow proper condenser operation.

The MCIMX53SMD board was designed to be used with a range of microphone options, including the mono-microphone/earbud sets commonly used with cellular phones. For this reason, the microphone bias voltage is connected to the microphone input signal on the MCIMX53SMD board, rather than connecting the bias voltage signal to a separate channel on the Microphone Jack (J6) and allowing a higher end microphone to connect the bias source closer to the connector. In addition, the right channel audio output of the Audio CODEC can be sent to the Microphone Jack. The MCIMX53SMD board does not come with this feature by default, but the developer can easily populate the L22 footprint with a ferrite bead or a 0Ω jumper.

The MCIMX53SMD board is also designed with a cable detect feature on both the Headphone and Microphone Jacks. One option would be to use an audio connector with an internal flag that would make or break depending on whether the connector barrel was inserted into the jack. These connectors are available, but are often more expensive and may have supply problems. On the MCIMX53SMD board, a four pin, Audio/Video style connector was chosen to implement the cable detect feature. When a three connector cable is inserted into the connector, the cable detect pin is shorted to the ground pin, sending an active low signal back to the processor to indicate that a cable was inserted. For this reason, the ground pin on the Microphone and Headphone Jacks must be system ground and not a virtual audio ground. Therefore, the Audio CODEC was designed to use the AC Coupled audio mode which makes use of two 220 µF capacitors. If the developer wishes to design a board that uses a flagged jack for cable detection or does not implement a cable detection scheme, it would then be possible to use the Direct Drive feature of the Audio CODEC and eliminate the need for large capacitors.

The Audio CODEC can be reset by software through the I2C channel, but there is no hardware reset pin on the CODEC. Should I2C communications be lost between the Audio CODEC and the Processor, it may be necessary to shut down DCDC_3V3_BB power to the MCIMX53SMD board and reinitialize the Audio CODEC by the power up sequence.

A power amplifier (TS4984IQT) and a 2-channel speaker are added to the MCIMX53SMD board. The TS4984IQT amplifier has been designed for top-class stereo audio applications. Due to its compact and power dissipation efficient QFN package, it can be used in a variety of applications. With a BTL configuration, this Audio Power Amplifier can deliver 1W per channel of continuous RMS output power into an 8Ω load at 5V. An externally controlled pin can be configured to reduce the supply current to less than 10 nA per channel. The device also features an internal thermal shutdown protection. The gain of each channel can be configured by external gain setting resistors.

5.12. Ethernet (Debug Board)

The Ethernet subsystem of the MCIMX53SMD board is provided by the SMSC LAN8720 Ethernet Transceiver (U17). The Ethernet Transceiver (or PHY) receives standard RMII Ethernet signals from the Fast Ethernet Controller (FEC) of the i.MX53 processor. The processor takes care of all Ethernet protocols at the MAC layer and higher layers. The PHY is responsible only for the Link Layer formatting. The PHY receives a 50 MHz clock signal from the oscillator X1. On initial versions of the i.MX53 silicon, this clock signal was shared with the SATA module of the i.MX53 processor. On current versions of the MCIMX53SMD board, the 50 MHz clock

signal is only sent to the Ethernet PHY. The two control traces from the i.MX53 processor to the Ethernet PHY are: an active low interrupt trace (FEC_nINT) and an active low reset line (FEC_nRST). When the PHY comes out of reset, it is internally programmed to establish communications with an attached Ethernet device and is ready to correctly format all communications being transmitted or received by the processor. If communications become unreliable, the processor can restart the PHY by forcing it into reset.

The PHY is connected to debug connector (J127) through a magnetic device. It has two pairs of differential traces for receive and transmit. The differential pair traces are biased externally with 49.9 1%Ω pull-up resistors. When initially connected to another Ethernet device, the PHY will negotiate to determine if it is connected to a switch type device or another Ethernet end device, and will reconfigure the Transmit and Receive inputs to correctly match the device attached. This eliminates the need for cross-over cables when directly connecting to another Ethernet end device. The LED status indicators are driven by the PHY to show a connected link and activity on the link. It is important to note that the LED control lines from the PHY also serve as PHY feature selection options. At boot time, the LED1 control pin determines whether the 1.2V internal regulator should be turned ON or OFF, and the LED2 control pins determines whether the PHY accepts an external reference clock or internally generates the clock signal and outputs it to the processor for reference. See the LAN8720 data sheet for more details.

5.13. USB PHY Connections

The i.MX53 processor has two internal USB PHY: one for USB HOST and other for USB OTG. The USB OTG connected to the MCIMX53SMD board signals with micro-B USB connector directly. For the USB HOST, it is connected with a USB-HUB, USB2514, from SMSC. The SMSC 4-Port HUB is low power, OEM configurable, MTT hub controller IC with four downstream ports for embedded USB solutions.

The 4-port hub is fully compliant with the USB2.0 Specification and will attach to an upstream port as a Full-Speed Hub or as a Full-/High-Speed Hub. The 4-Port Hub supports Low-Speed, Full-Speed, and High-Speed (if operating as a High-Speed Hub) downstream devices on all the enabled downstream ports. Two of four USB ports (Port1 and Port4) are dedicated to USB HOST Connector. Port2 is dedicated to 3G Modem on the MCIMX53SMD board and Port3 is for VGA Dock connector. The MCIMX53SMD board uses a USB power switch for Port1 and Port4. Each one can provide 500 mA current, and over current interrupt will occur when high current happened. Meanwhile, we use the same chip for USB OTG.

5.14. SATA

The internal SATA PHY of the i.MX53 processor provides the two differential pair data signals necessary for SATA operations. No external transceiver is required. Each of the four data lines pass through a 0.01 µF capacitor for decoupling. These capacitors are placed as close to the SATA connector as possible. The Processor SATA module receives 2.5V power from VBUCKPERI for the PHY portion of the module and 1.3V power from VLDO5_1V3 for the controller portion of the module. A 191Ω 1% resistor must be connected to the SATA_REXT pin (C13). This resistor received a small, constant current at the initialization of the SATA module to allow cable impedance calibration. This resistor is not required after module initialization.

The i.MX53 processor provides two pins to receive an external differential pair clock input to be used by the SATA module. Testing of the i.MX53 processor confirms that the internally generated clock signal is working properly. Therefore, the external clock components are not populated and the eFUSEs for the processor are configured for internal clock operation.

The SATA connector is suitable to be used with all SATA capable storage media devices, including Hard Drives and Optical Media storage devices (DVD/CD). We use SSD SATA on the MCIMX53SMD board, by default. It is possible to configure the MCIMX53SMD board to boot directly from a SATA device. To enable the MCIMX53SMD board to boot from SATA, the developer needs to set SW26 to 01010000.

5.15. Debug UART Serial Port (Debug Board)

The i.MX53 processor has five independent UART Ports (UART1 – UART5). By default, the processor will boot using UART1 to output serial debugging information, specifically on pins CSI0_DAT10 (pin R5) and CSI0_DAT11 (pinT2). These two pins are outputted from the NVCC_CSI module, which is pulled up to 1.8V on the MCIMX53SMD board. The MCIMX53SMD board uses two single-direction level shifters (U40, U41) to convert the UART Transmit and Receive signal to a 3.3V logic signal. The level shifted signals are sent to a low cost, RS232 transceiver, which reformats the signals to the correct voltages and drives the signals. The resulting cable ready signals are then connected to the RS232 Debug connector. No RTS or CTS signals are sent from the processor to the Debug connector, since these signals are commonly ignored by most applications. The required terminal settings to receive debug information during the boot cycle are shown in **Table 5-7**.

Data Rate	115,200 Baud
Data bits	8
Parity	None
Stop bits	1
Flow Control	None

Table 5-7. Terminal Setting Parameters

If the developer wishes to use the Debug UART connector in software as an Applications Connector, the MCIMX53SMD board can support this using a Null Modem Adapter. The adapters are readily available from most cable and electronics stores at a low cost.

5.16. JTAG Operations (Debug Board)

The i.MX53 processor accepts five JTAG signals from an attached debugging device on dedicated pins. A sixth pin on the processor accepts a HW board configured input, specific to the MCIMX53SMD board. The five JTAG signals used by the processor are:

- JTAG_TCK TAP Clock
- JTAG_TMS TAP Machine State
- JTAG_TDI TAP Data In
- JTAG_TDO TAP Data Out
- JTAG_nTRST TAP Reset Request (Active Low)

The TAP Clock signal is provided by the attached debugging device that serves as a reference for data exchange between the debugging device and the processor. The TAP Machine State is a logical signal provided by the debugging device to let the processor (or target) know which state to enter next. As per JTAG specifications, there are two states, one of which can be selected with a ‘high’ signal and other with a ‘low’ signal. The TAP Data In and TAP Data Out signals are used only for data transfer.

The Active Low TAP Reset Request is initiated by the debugging device and it resets the TAP (JTAG) module within the processor. This enables the debugging device to reset the internal processor JTAG module, if required, without affecting rest of the processor. The system JTAG reset signal provided by the attached debugging device does not go to the JTAG module of the processor, but goes to the external processor reset circuitry. This will reset the entire i.MX53 processor, but not the power rails.

The JTAG_MOD pin used by the JTAG module of the i.MX53 processor determines what portion of the i.MX53 processor is connected to the JTAG debugging device. In the pull-down mode (default on the MCIMX53SMD board), all the i.MX53 TAPs (SJC, SDMA, ARM) are connected to the debugging device in a daisy chain connection. If the JTAG_MOD pin is pulled high, then, the attached debugging device can only access the SJC TAP.

Three other common JTAG signals used by debugging devices (Return Clock, Data Enable, and Data Acknowledge) are not used by the i.MX53 processor and are either pulled-up or pulled-down by the MCIMX53SMD board.

On the MCIMX53SMD board, the logic signals for JTAG are designed to be 1.8V. A 1.8V reference signal from VLDO8_1V8 is connected to pin 1 of the 20-pin JTAG connector to provide this logic level signal to the attached debugging device. In addition, a limited amount (~0.5A) of 3.3V power can be supplied to the debugging device for debugging devices that required power.

5.17. CMOS Sensor

The MCIMX53SMD board includes a 500 Megapixel CMOS Camera, OV5642, by OmniVision. The i.MX53 processor can configure the OV5642 registers through I2C port, and get the value from an 8-bit data interface. The MCIMX53SMD board does not support AF function. The developer can use another CMOS module, but must follow the pin map of the connector. The MCIMX53SMD board uses FX12B-40P-0.4SV from HIROSE.

5.18. Sensors

The MCIMX53SMD board has four sensors: Accelerometer (MMA8452), eCOMPASS (MAG3112), CAP Touch Sensor (MRP121), and Light Sensor (ISL29023). These four sensors are connected with three i.MX53 I2C ports: Accelerometer is connected with I2C1 port, eCOMPASS and CAP Touch Sensor are connected with I2C2 port, and Light Sensor is connected with I2C3 port.

6.18.1. Accelerometer

Accelerometer, MMA8452, is an intelligent low power and lower noise, 3 x 3 x 1 mm capacitive micro-machined accelerometer having 12 bits of resolution. This accelerometer is packed with many flexible user programmable embedded functions that are available with two configurable interrupt pins. MMA8452 has user selectable full scales of ±2g/±4g/±8g and it is capable of measuring accelerations with an Output Data Rate (ODR) of 400 Hz, 200 Hz, 100 Hz, 50 Hz, 12.5 Hz, and 1.563 Hz. These output data rates correspond to sample intervals from 2.5 ms to 640 ms. The device can be configured to generate inertial wake-up interrupt signals, when a programmable acceleration threshold is crossed on any of the three sensed axes. Acceleration and time thresholds of interrupt generators are programmable by the end user.

6.18.2. eCOMPASS

eCOMPASS, MAG3112, is a small, low-power, 3-axis digital magnetometer. It works by measuring the strength of a magnetic field, which is a combination of earth's magnetic field and the magnetic fields of the nearby objects, including distortions. The device can be used in conjunction with a 3-axis accelerometer to produce orientation-independent, accurate compass heading information. It features a standard I2C serial interface output and smart embedded functions.

6.18.3. CAP Touch Sensor

CAP Touch Sensor, MPR121, is the second generation sensor controller after the initial release of the MPR03x series devices. The MPR121 features increased internal intelligence in addition to Freescale's second generation capacitance detection engine. Some of the major additions include an increased electrode count, a hardware configurable I2C address, an expanded filtering system with debounce, and completely independent electrodes with built-in auto configuration. The total number of electrodes is 13, including 12 physical electrodes and one electrode for proximity detection. Only four electrodes pad on the MCIMX53SMD board: electrodes for "HOME","BACK","SEARCH", and "ENTER".

6.18.4. Light Sensor

Light Sensor, ISL29023, is an integrated ambient and infrared light to digital converter with I2C (SMBus Compatible) Interface. Its advanced self-calibrated photodiode array emulates human eye response with excellent IR rejection. The on-chip ADC is capable of rejecting 50 Hz and 60 Hz flicker caused by artificial light sources. The lux range select feature allows users to program the lux range for optimized counts/lux. For ambient light sensing, an internal 16-bit ADC has been designed by using the charge-balancing technique. The nominal ADC conversion time is 90 ms; however, the user can adjust it between 11 µs to 90 ms, depending on the oscillator frequency and ADC resolution.

5.19. 3G Modem

The MCIMX53SMD board has a mini-PCIe interface that can be used by 3G modem. The developer can use USB port to communicate with 3G modem. No A/D audio interface is reserved for 3G modem. The developer needs to have a 3G modem, no 3G modem is provided with the MCIMX53SMD board kit.

5.20. WiFi/BT Module

The MCIMX53SMD board also has another mini-PCIe interface that can be used by the WiFi/BT module. The WiFi/BT module is designed by a Taiwan-based company, USI, which has Atheros as one of its major chipset providers.

This is a half size mini card featured with steady stream of up to 150 Mbits/s wireless networking and Bluetooth combo function to provide both technologies for enterprise and home wireless LAN and PAN access. The half size mini card is based on the Atheros AR6003 and AR3001 integrated circuits. AR6003 supports 802.11a, 11b, 11g, and multimode 11n WLAN implementations. AR3001 provides a highly integrated, complete Bluetooth system, and it is compliant with latest Bluetooth V2.1+EDR specification. A firmware-based architecture can support latest industry standards in the security and quality of service (QoS), draft 802.11i and 802.11e (WMMTM) standards, respectively.

Note that this PCIe connector pin-map is just mapped to Atheros WiFi/BT module, which uses a non standard mini-PCIe pin map. No other mini-PCIe card should be connected to this slot.

The i.MX53 processor controls WiFi part through SDIO port. A 4-line UART and an I2S are connected with BT part.

5.21. GPS Module

The MCIMX53SMD board also has GPS module, GM22, which uses AR1520A. The AR1520A is a monolithic, highly-integrated, 130 nm CMOS single-chip GPS receiver that combines the functionality of a single-conversion GPS RF front-end and GPS baseband processor. A complete GPS receiver built with the AR1520A needs only a handful of external components, such as SAW filter, TCXO, RTC crystal, and few passive components, keeping the overall bill of materials to a minimum. Many peripherals, controlled by CPU, support I/O that can be configured on any of the GPIO pins. The device features multiple power islands, 1.8/3V I/O compatibility, battery backup RTC, on-chip regulators, and powerful GPS specific functions.

The i.MX53 processor controls the GPS module through UART.

5.22. ZigBee

The MCIMX53SMD board uses MC1323x as ZigBee function. The MC1323x family is Freescale's low cost SoC platform for the IEEE® 802.15.4 standard. It incorporates a complete, low power, 2.4 GHz radio frequency transceiver with transmit/receive switch, an 8-bit HCS08 CPU, and a functional set of MCU peripherals into a 48-pin LGA package. This family of products is targeted for wireless RF remote control and other cost-sensitive

applications ranging from home TV and entertainment systems, such as ZigBee BeeStack Consumer (RF4CE), to low cost, low power, IEEE 802.15.4 and ZigBee end nodes. The MC1323x is a highly integrated solution, with very low power consumption. The MC1323x contains an RF transceiver, which is an 802.15.4 Standard - 2006 compliant radio that operates in the 2.4 GHz ISM frequency band. The transceiver includes a low noise amplifier, 1 mW nominal output power amplifier (PA), internal voltage controlled oscillator (VCO), integrated Tx/Rx switch, on-board power supply regulation, and full spread-spectrum encoding and decoding.

The i.MX53 processor controls ZigBee through CSPI and I2C.

6. Connector Pin-Outs

This section describes the signals going to each of the 14 types of connectors used on the MCIMX53SMD board. Although this information is available on the schematic, the footprint used in manufacturing the PCB is also included to provide a map to the actual signals on the board. The image of the footprint provides its top view. In addition to the pin tables and footprints, there is also a pin-mux table provided for the Expansion Port so that the developer can readily see the possible signals brought out through the Expansion Port. These details are included in the following tables and figures:

Power Jack (J35)

Positive Terminal	1
Negative Terminal	2
Ground Terminal	3

Table 6-1. Power Jack (J35)

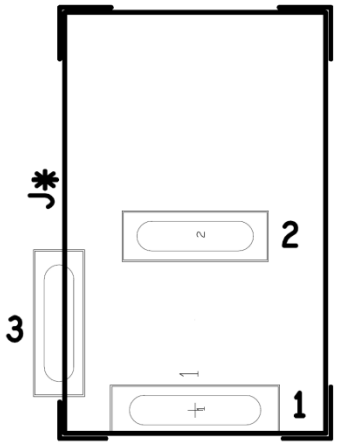


Figure 6-1. Power Jack (J35)

Micro-B USB (J34)

5V Power	1
Data Negative	2
Data Positive	3
No Connect (ID)	4
Ground	5
Chassis Ground	6
Chassis Ground	7
Chassis Ground	8
Chassis Ground	9
Chassis Ground	10
Chassis Ground	11

Table 6-2. Micro-B USB Connector (J34)

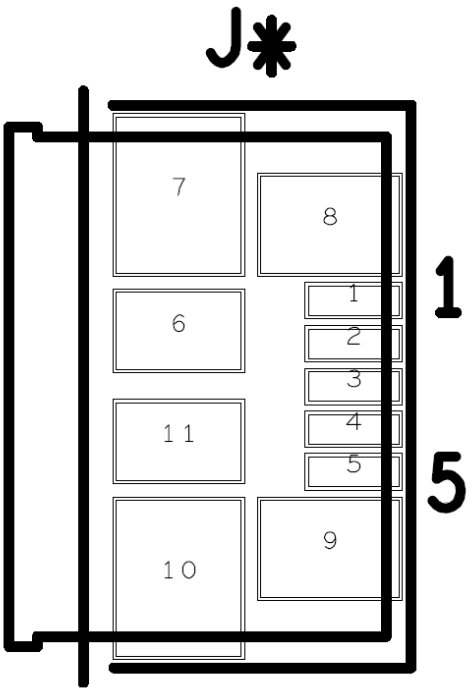


Figure 6-2. Micro-B USB Connector (J34)

USB (J31, J32)

USB 5V Power	A1
USB Data Negative	A2
USB Data Positive	A3
USB Ground	A4
Shield Ground	S1
Shield Ground	S2

Table 6-3. USB HOST Connector (J31, J32)

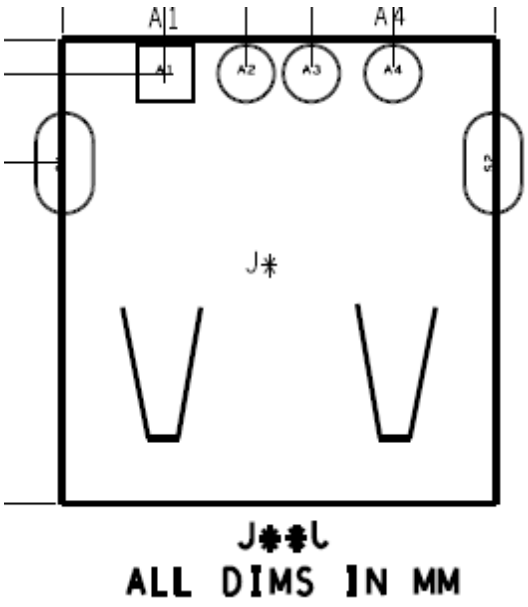


Figure 6-3. USB HOST Connector (J31, J32)

Headphone Connector (J130)

Right channel	1
Left Channel (Tip)	4
Analog Ground (Ring)	5
Plug Sense	6

Table 6-4. Headphone Connector (J130)

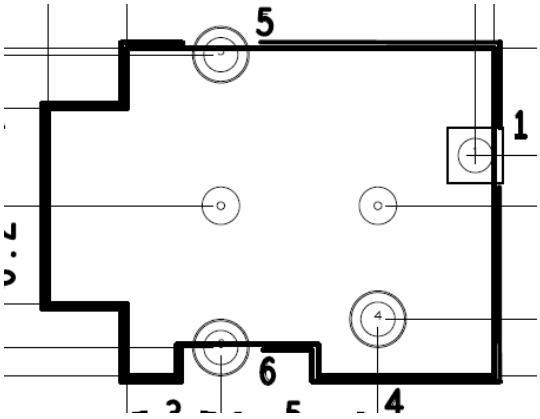


Figure 6-4. Headphone Connector (J130)

CMOS Camera Connector (J12)

1	GND	GND	2
3	No Connect	1.8V Power	4
5	IIC Data	Pull-up to 1.8V	6
7	IIC Clock	2.75V Power	8
9	CMOS Reset	No Connect	10
11	CSI0_PIXCLK	No Connect	12
13	CSI0_VSYNC	GND	14
15	CSI0_HSYNC	No Connect	16
17	CMOS Power Down	No Connect	18
19	CSI0_DAT19	GND	20
21	CSI0_DAT18	No Connect	22
23	CSI0_DAT17	No Connect	24
25	CSI0_DAT16	GND	26
27	CSI0_DAT15	No Connect	28
29	CSI0_DAT14	No Connect	30
31	CSI0_DAT13	GND	32
33	CSI0_DAT12	CSI0_MCLK	34
35	No Connect	1.5V Power	36
37	No Connect	1.8V Power	38
39	GND	GND	40
41	GND	GND	42
43	GND	GND	44
45	Shield Ground	Shield Ground	46

Table 6-5. CMOS Camera Connector (J12)

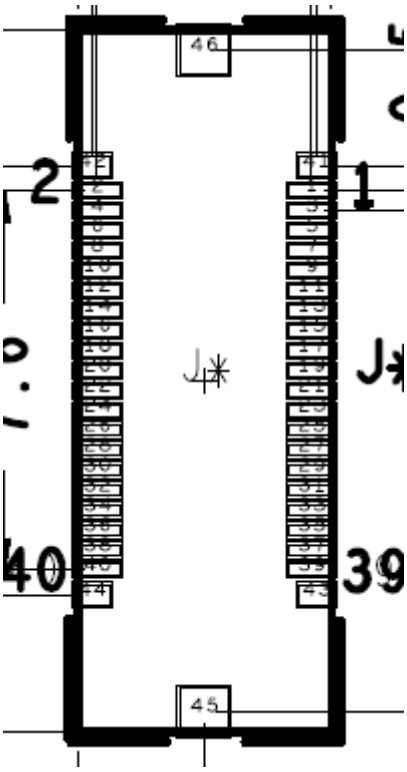


Figure 6-5. CMOS Camera Connector (J12)

HDMI Mini Connector (J25)

GND	1
HDMI Data2 Positive	2
HDMI Data2 Negative	3
GND	4
HDMI Data1 Positive	5
HDMI Data1 Negative	6
GND	7
HDMI Data0 Positive	8
HDMI Data0 Negative	9
GND	10
HDMI Clock Positive	11
HDMI Clock Negative	12
GND	13
CEC	14
EDID Clock	15
EDID Data	16
No Connect	17
5V Power	18
Hot Plug Detect	19
Shield Ground	20
Shield Ground	21
Shield Ground	22
Shield Ground	23

Table 6-6. HDMI Mini Connector (J25)

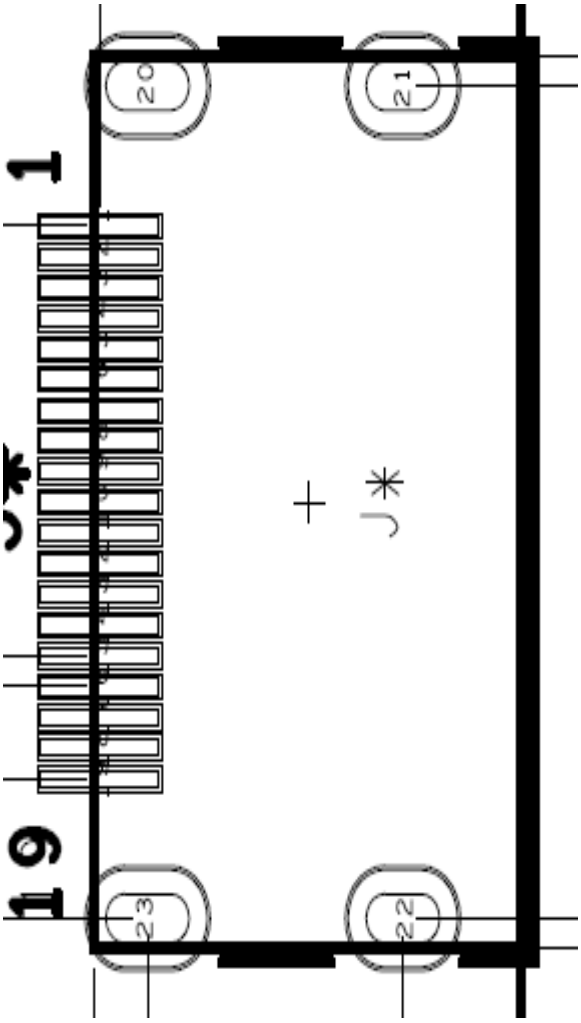


Figure 6-6. HDMI Mini Connector (J25)

SATA Connector (J5)

Ground	S1
Transmit Data Positive	S2
Transmit Data Negative	S3
Ground	S4
Receive Data Negative	S5
Receive Data Positive	S6
Ground	S7
3.3V Power	P1
3.3V Power	P2
3.3V Power	P3
Ground	P4
Ground	P5
Ground	P6
5V Power	P7
5V Power	P8
5V Power	P9
Ground	P10
No Connect	P11
Ground	P12
No Connect	P13
No Connect	P14
No Connect	P15

Table 6-7. SATA Connector (J5)

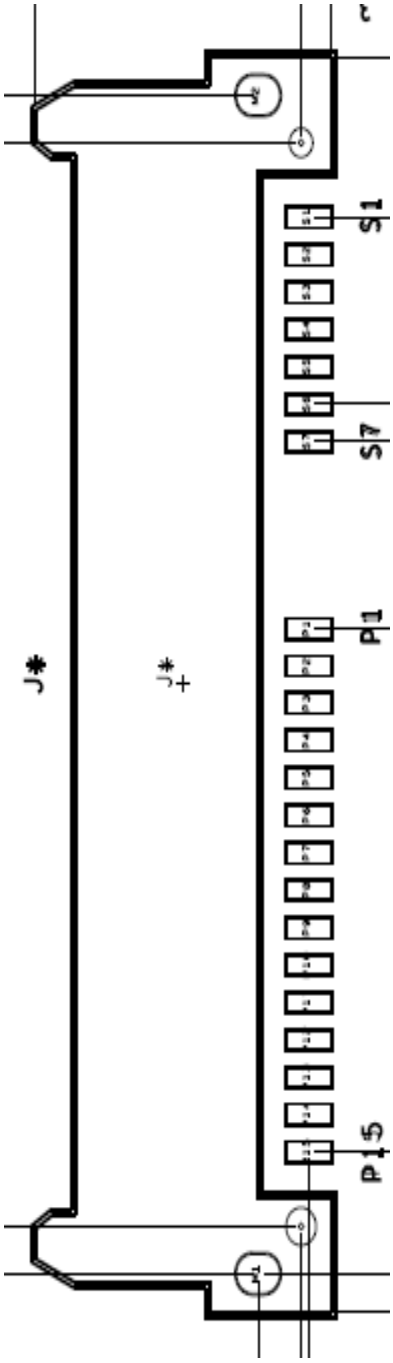


Figure 6-7. SATA Connector (J5)

LVDS Connector (J28, J29)

Backlight Enable	1
3.3V Power	2
3.3V Power	3
3.3V Power	4
LED Brightness Adjust	5
EDID I2C (Clock)	6
EDID I2C (Data)	7
LVDS Transmit 0 Negative	8
LVDS Transmit 0 Positive	9
Ground	10
LVDS Transmit 1 Negative	11
LVDS Transmit 1 Positive	12
Ground	13
LVDS Transmit 2 Negative	14
LVDS Transmit 2 Positive	15
Ground	16
LVDS Clock Negative	17
LVDS Clock Positive	18
Ground	19
Touch Panel 5V Supply	20
Touch Panel 5V Supply	21
Ground	22
Ground	23
LED 5V Supply	24
LED 5V Supply	25
LED 5V Supply	26
Touch I2C (Clock)	27
Touch I2C (Data)	28
Touch I2C Interrupt	29
Touch Function	30

Table 6-8. LVDS Connector (J28, J29)

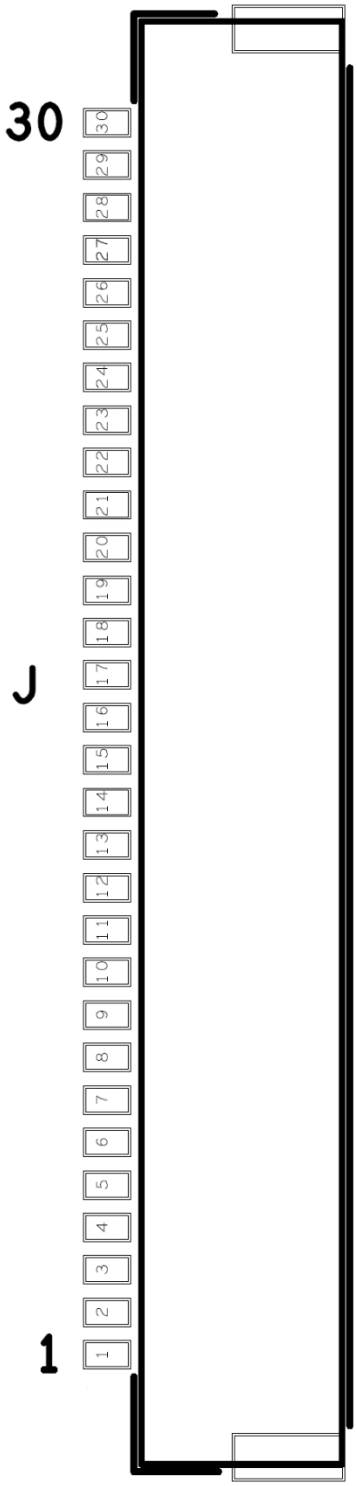


Figure 6-8. LVDS Connector (J28, J29)

SD Card Connector (J13)

Data3	1
Command	2
Ground	3
3.3V Power	4
Clock	5
Ground	6
Data0	7
Data1	8
Data2	9
No Connect	10
No Connect	11
No Connect	12
No Connect	13
Card Detect	14
Write Protect	15
Shield Ground	16
Shield Ground	17
Shield Ground	18
Shield Ground	19

Table 6-9. SD Card Connector (J13)

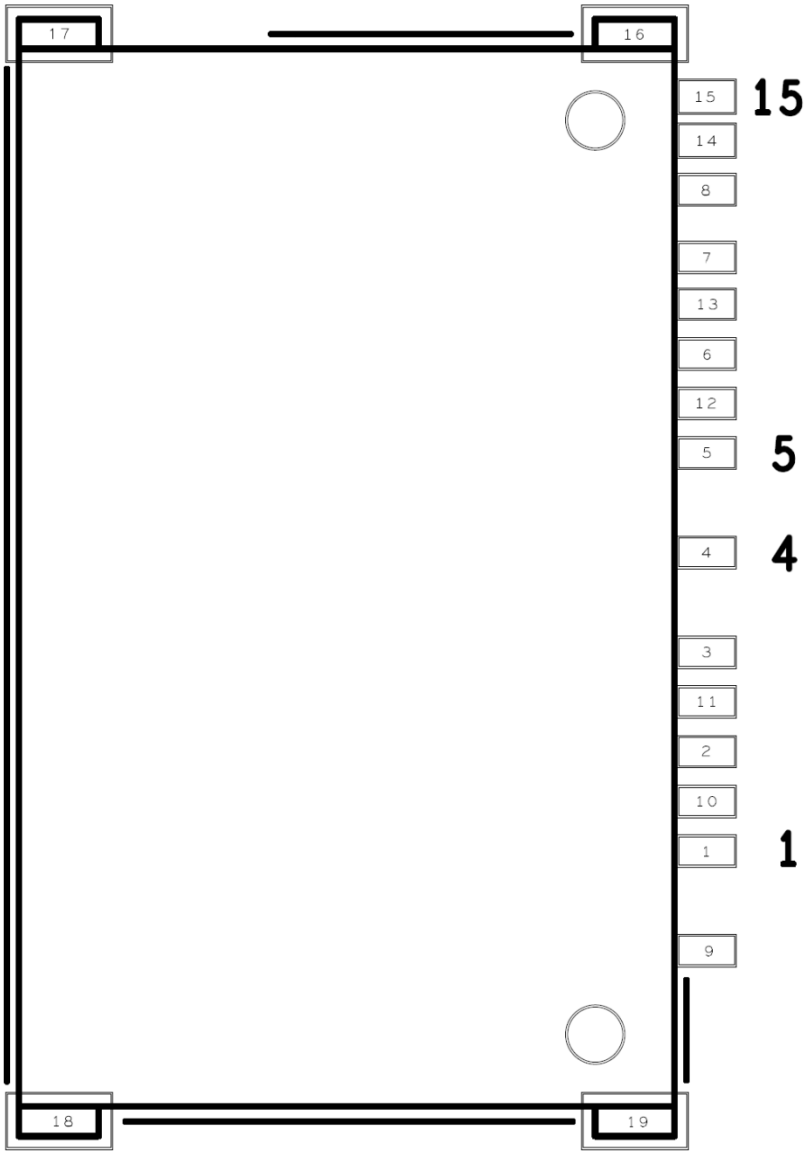


Figure 6-9. SD Card Connector (J13)

Mini-PCIe for WiFi/BT Connector (J15)

1	3.3V Power	3.3V Power	2
3	3.3V Power	3.3V Power	4
5	No Connect	GND	6
7	No Connect	GND	8
9	GND	3.3V Power	10
11	1.8V Power	3.3V Power	12
13	GND	GND	14
15	No Connect	No Connect	16
17	No Connect	No Connect	18
19	No Connect	No Connect	20
21	WLAN HOST WAKE	WLAN PD	22
23	WLAN SD DAT0	GND	24
25	WLAN SD CLK	GND	26
27	WLAN SD DAT1	WLAN SD DAT2	28
29	WLAN SD CMD	WLAN SD DAT3	30
31	No Connect	3.3V Power	32
33	BT_PCM_OUT	BT_PCM_IN	34
35	BT_PCM_BCK	BT_PCM_SYNC	36
37	BT_PCM_MCK	No Connect	38
39	No Connect	No Connect	40
41	BT_ACTIVE	BT RESET	42
43	BT HOST WAKE	BT_UART_CTS	44
45	BT_UART_RTS	BT_UART_RXD	46
47	BT_UART_TXD	GND	48
49	WLAN ACTIVE	GND	50
51	BT PRIORITY	GND	52

Table 6-10. Mini-PCIe for WiFi/BT Connector (J15)

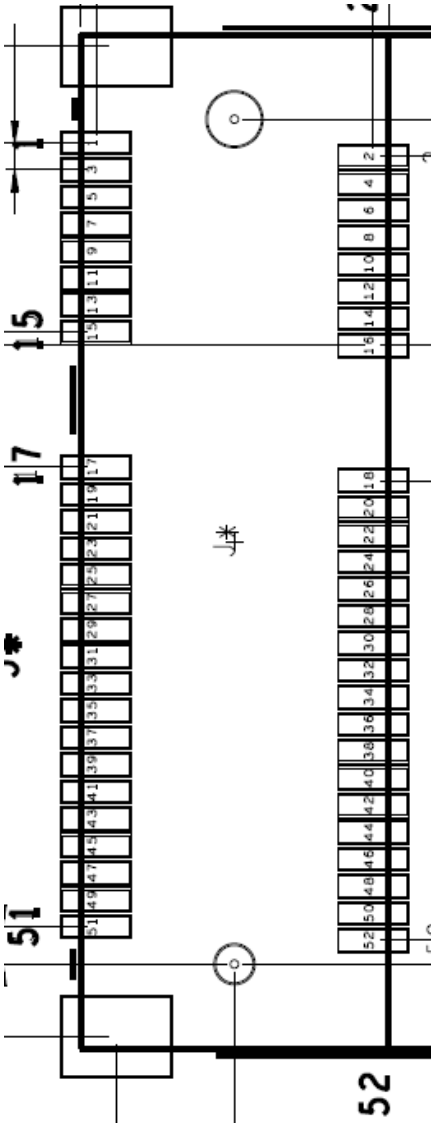


Figure 6-10. Mini-PCIe for WiFi/BT Connector (J15)

Mini-PCIe for 3G Connector (J18)

1	Modem Wake Up	3.3V Power	2
3	No Connect	GND	4
5	No Connect	No Connect	6
7	No Connect	SIM Power	8
9	GND	SIM IO	10
11	Test Point	SIM CLK	12
13	Test Point	SIM RESET	14
15	GND	SIM VPP	16
17	Test Point	GND	18
19	Test Point	Modem Disable	20
21	GND	Modem Reset	22
23	No Connect	3.3V Power	24
25	No Connect	GND	26
27	GND	No Connect	28
29	GND	No Connect	30
31	No Connect	No Connect	32
33	No Connect	GND	34
35	GND	USB Data-	36
37	No Connect	USB Data+	38
39	GND	GND	40
41	GND	WWAN LED	42
43	No Connect	No Connect	44
45	No Connect	No Connect	46
47	No Connect	No Connect	48
49	No Connect	GND	50
51	No Connect	3.3V Power	52

Table 6-11. Mini-PCIe for 3G Connector (J18)

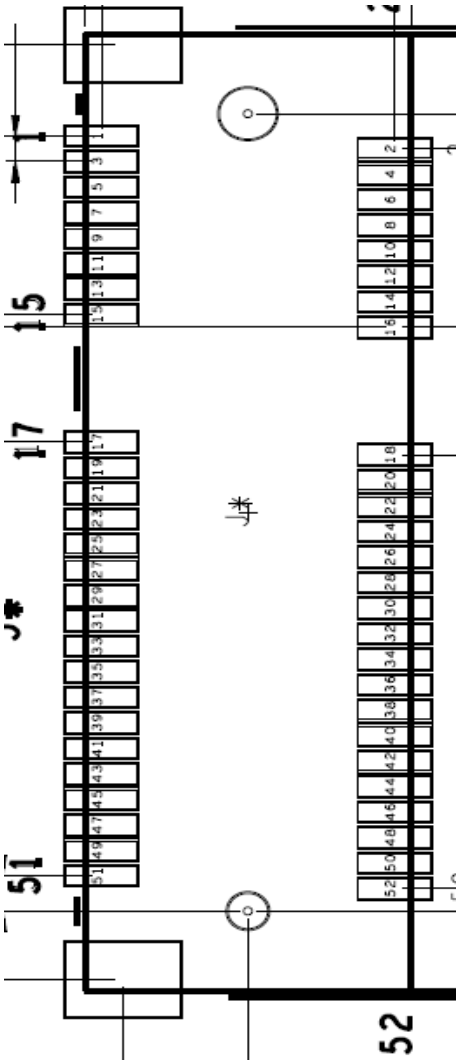


Figure 6-11. Mini-PCIe for 3G Connector (J18)

Debug Connector (J127)

RS232 TXD	1
GND	2
GND	3
JTAG TDI	4
RS232 RXD	5
JTAG TDO	6
1.8V Power	7
GND	8
3.3V Power	9
JTAG TCK	10
JTAG TRST	11
JTAG TMS	12
JTAG SRST	13
GND	14
RESET	15
No Connect	16
No Connect	17
No Connect	18
GND ENET	19
Eth RXN0	20
ENET_LINKLED	21
No Connect	22
ENET_100MLED	23
No Connect	24
No Connect	25
Eth RXP0	26
5V Power	27
Eth TXN0	28
GND ENET	29
Eth TXP0	30

Table 6-12. Debug Connector (J127)

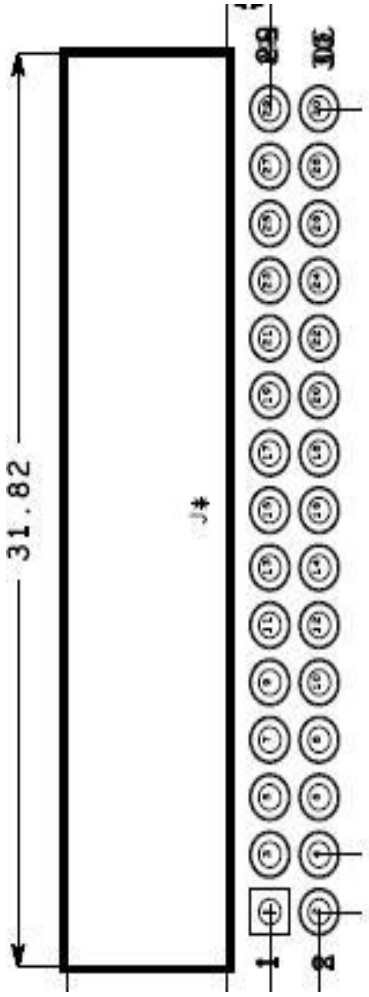


Figure 6-12. Debug Connector (J127)

VGA Dock (J131)

1	GND	GND	2
3	Right Line Out	Right Line In	4
5	Left Line Out	Left Line In	6
7	GND	GND	8
9	No Connect	VGA EDID Data	10
11	No Connect	VGA EDID Clock	12
13	3.3V Power	GND	14
15	SYS EJECT	VGA VSYNC	16
17	ON/OFF Sleep Wake	VGA HSYNC	18
19	Dock Detect	VGA GND	20
21	GND	IOR	22
23	1.8V Power	IOG	24
25	3.3V Power	VGA GND	26
27	5V Power	IOB	28
29	GND	GND	30
31	GND	USB Data-	32
33	15V Power	USB Data+	34
35	15V Power	GND	36
37	No Connect	No Connect	38
39	No Connect	No Connect	40
41	No Connect	No Connect	42
43	No Connect	No Connect	44

Table 6-13. VGA Dock (J131)

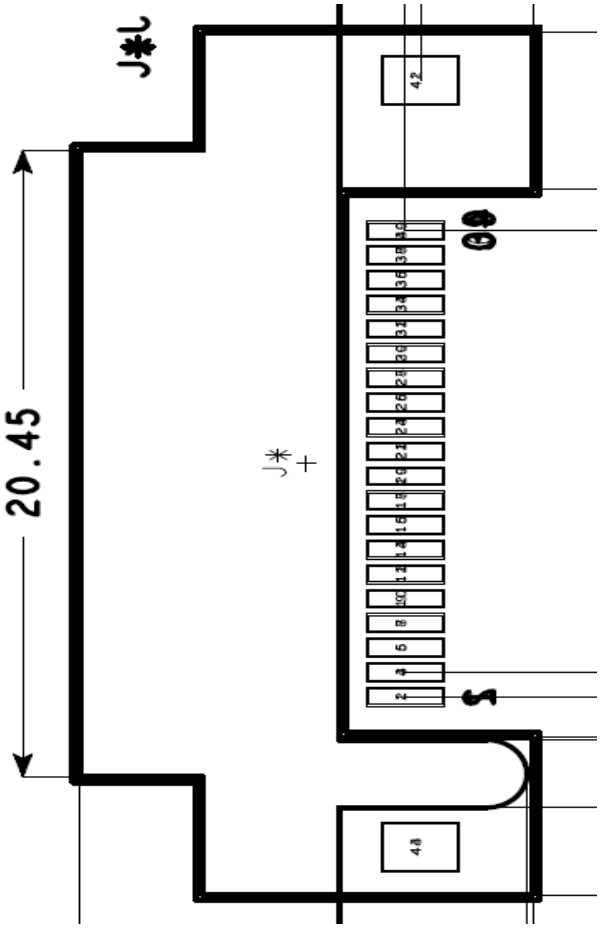
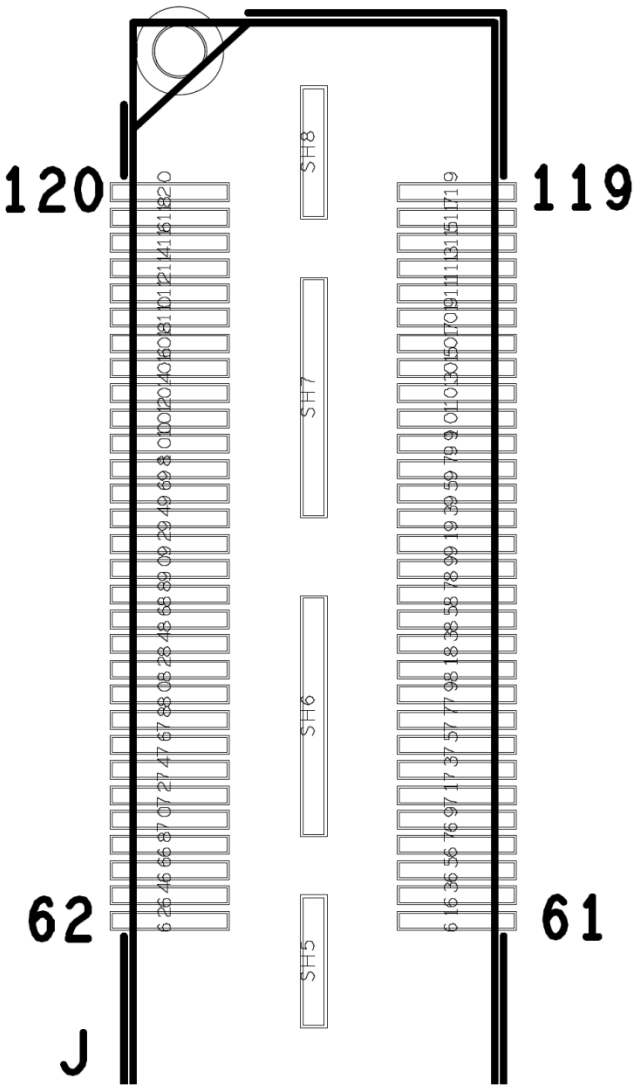


Figure 6-13. VGA Dock (J131)

Expansion Port Connector (J78)

SH8	Shield Ground	Shield Ground	SH7
120	No Connect	No Connect	119
118	No Connect	Display Read	117
116	Display Data Ready	1.5V Power (VLDO9)	115
114	Display Horiz Synch	1.5V Power (VLDO9)	113
112	Backlight Brightness Adj	1.5V Power (VLDO9)	111
110	Display Vert Synch	Display Write	109
108	Display Data23	Disp Chip Sel1 (Act Low)	107
106	Display Data22	Disp Chip Sel0 (Act Low)	105
104	Display Data21	Ground	103
102	Display Data20	Touch Screen X-Neg	101
100	Display Data19	Touch Screen X-Pos	99
98	Display Data18	Touch Screen Y-Neg	97
96	Display Data17	Touch Screen Y-Positive	95
94	Display Data16	Ground	93
92	Display Data15	IIS Reset	91
90	Display Data14	IIS Clock	89
88	Display Data13	IIS Master Out-Slave In	87
86	Display Data12	IIS Master In-Slave Out	85
84	Display Data11	Exp Card ID1	83
82	Display Data10	IIS Chip Sel (Active Low)	81
80	Display Data09	Display Power Enable	79
78	Display Data08	5V Power	77
76	Display Data07	5V Power	75
74	Display Data06	5V Power	73
72	Display Data05	No Connect	71
70	Display Data04	No Connect	69
68	Display Data03	No Connect	67
66	Display Data02	No Connect	65
64	Display Data01	Audio System Clock	63
62	Display Data00	Exp Card ID0	61
SH6	Shield Ground	Shield Ground	SH5



Expansion Port Connector (J78)

SH4	Shield Ground	Shield Ground	SH3
60	Ground	Display Rst (Active Low)	59
58	Display Vert Synch	No Connect	57
56	Display Horiz Synch	No Connect	55
54	Ground	Display Power Down	53
52	Display Data19	No Connect	51
50	Display Data18	3.2V Power	49
48	Ground	3.2V Power	47
46	Display Data17	3.2V Power	45
44	Display Data16	Display Data Clock	43
42	Ground	No Connect	41
40	SPDIF Data Transmit	No Connect	39
38	SPDIF Data Clock	No Connect	37
36	Ground	Display Pixel Clock	35
34	Display Data15	Display Reset	33
32	Display Data14	I2C Clock	31
30	Ground	I2C Data	29
28	Display Data13	No Connect	27
26	Display Data12	1.8V Power (VLDO8)	25
24	Ground	No Connect	23
22	No Connect	No Connect	21
20	No Connect	1.8V Power (VLDO8)	19
18	Ground	1.8V Power (VLDO8)	17
16	No Connect	Display Backlight Return	15
14	No Connect	5V Power	13
12	Ground	5V Power	11
10	No Connect	Display Backlight Power	9
8	5V Power	5V Power	7
6	Ground	3.2V Power	5
4	5V Power	2.775V Power (VLDO4)	3
2	5V Power	1.8V Power (VLDO8)	1
SH2	Shield Ground	Shield Ground	SH1

Table 6-14. Expansion Port (J78)

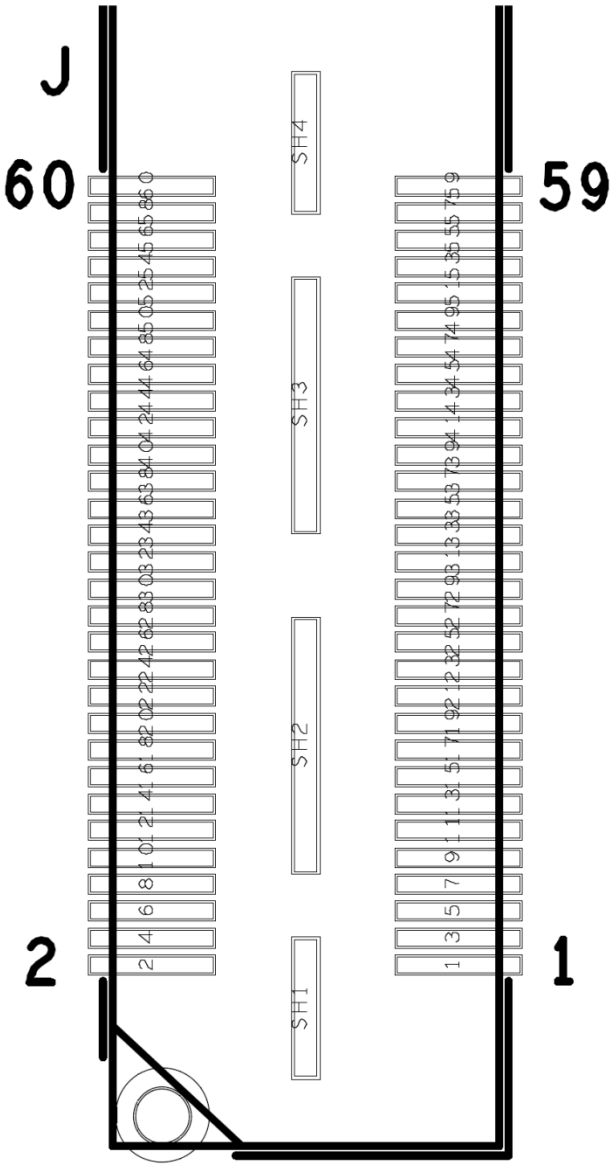


Figure 6-14. Expansion Port (J78)

J78 PIN	J13 Name	i.MX53 Pin Name	ALT(1)	ALT(2)	ALT(3)
26	CSI0_DAT12	CSI0_DAT12	GPIO5_30	uart4 TXD_MUX	
28	CSI0_DAT13	CSI0_DAT13	GPIO5_31	uart4 RXD_MUX	
29	I2C2_SDA	KEY_ROW3	GPIO4_13	H2_DP	ASRC_EXT_CLK
31	I2C2_SCL	KEY_COL3	GPIO4_12	H2_DM	spdif IN1
32	CSI0_DAT14	CSI0_DAT14	GPIO6_0	uart5 TXD_MUX	
33	DISP0_RESET	EIM_WAIT	GPIO5_0	WEIM_DTACK_B	
34	CSI0_DAT15	CSI0_DAT15	GPIO6_18	uart5 RXD_MUX	
35	CSI0_PIXCLK	CSI0_PIXCLK	GPIO5_18		
38	PCLOCK	GPIO_7	GPIO1_7	EPITO	can1 TXCAN
40	SPDIF_TX	GPIO_17	GPIO1_12	SDMA_EXT_EVENT0	PMIC_RDY
43	DISP0_DCLK	DI0_DISP_CLK	GPIO4_15	USBH2_DIR	
44	CSI0_DAT16	CSI0_DAT16	GPIO6_2	uart4 RTS	
46	CSI0_DAT17	CSI0_DAT17	GPIO6_3	uart4 CTS	
50	CSI0_DAT18	CSI0_DAT18	GPIO6_4	uart5 RTS	
52	CSI0_DAT19	CSI0_DAT19	GPIO6_5	uart6 CTS	
53	SCSI0_PWDN	NANDF_RB0	GPIO6_10		
56	CSI0_VSYNCH	CSI0_VSYNCH	GPIO5_21		
58	CSI0_HSYNCH	CSI0_MCLK	GPIO5_19	ccm CSI0_MCLK	
59	CSI0_RSTB	NANDF_WP_B	GPIO6_9		
62	DISP0_DAT0	DISP0_DAT0	GPIO4_21	cspi SCLK	USBH2_DAT0
63	GPIO_0(CLK0)	GPIO_0	GPIO1_0	KEY_COL5	SSI_EXT1_CLK
64	DISP0_DAT1	DISP0_DAT1	GPIO4_22	cspi MOSI	USBH2_DAT1
66	DISP0_DAT2	DISP0_DAT2	GPIO4_23	cspi MISO	USBH2_DAT2
68	DISP0_DAT3	DISP0_DAT3	GPIO4_24	cspi SS0	USBH2_DAT3
70	DISP0_DAT4	DISP0_DAT4	GPIO4_25	cspi SS1	USBH2_DAT4
72	DISP0_DAT5	DISP0_DAT5	GPIO4_26	cspi SS2	USBH2_DAT5
74	DISP0_DAT6	DISP0_DAT6	GPIO4_27	cspi SS3	USBH2_DAT6
76	DISP0_DAT7	DISP0_DAT7	GPIO4_28	cspi RDY	USBH2_DAT7
78	DISP0_DAT8	DISP0_DAT8	GPIO4_29	pwm1 PWMO	wdog1 WDOG_B

Legend

UART4	AUDMUX4	I2C1	ECSPI2	USBH2
UART5	AUDMUX5	I2C2	CSPI	SPDIF

Table 6-15. Expansion Port Pin-Mux Table

J78 PIN	J13 Name	ALT(4)	ALT(5)	ALT(6)	ALT(7)
26	CSI0_DAT12	USBH3_DATA0	DEBUG_PC6	EMI_DEBUG41	tpiu TRACE9
28	CSI0_DAT13	USBH3_DATA1	DEBUG_PC7	EMI_DEBUG42	tpiu TRACE10
29	I2C2_SDA	i2c2 SDA	32K_OUT	ccm PLL4_BYP	usb1 LINESTATE0
31	I2C2_SCL	i2c2 SCL	ecspi1 SS3	fec CRS	usb1 SIECLOCK
32	CSI0_DAT14	USBH3_DATA2	DEBUG_PC8	EMI_DEBUG43	tpiu TRACE11
33	DISP0_RESET				
34	CSI0_DAT15	USBH3_DATA3	DEBUG_PC9	EMI_DEBUG44	tpiu TRACE12
35	CSI0_PIXCLK		DEBUG_PC0	EMI_DEBUG29	
38	PCLOCK	uart2 TXD_MUX	firi RXD	spdifPLOCK	ccm PLL2_BYP
40	SPDIF_TX	CE_RTC_FSV_TRIG	spdif OUT1	SNOOP2	JTAG_ACT
43	DISP0_DCLK		DEBUG_CORE_STATE0	EMI_DEBUG0	usb1 AVALID
44	CSI0_DAT16	USBH3_DATA4	DEBUG_PC10	EMI_DEBUG45	tpiu TRACE13
46	CSI0_DAT17	USBH3_DATA5	DEBUG_PC11	EMI_DEBUG46	tpiu TRACE14
50	CSI0_DAT18	USBH3_DATA6	DEBUG_PC12	EMI_DEBUG47	tpiu TRACE15
52	CSI0_DAT19	USBH3_DATA7	DEBUG_PC13	EMI_DEBUG48	usb2 BISTOK
53	SCSI0_PWDN				usb1 VSTATUS3
56	CSI0_VSYNCH		DEBUG_PC3	EMI_DEBUG32	tpiu TRACE0
58	CSI0_HSYNCH		DEBUG_PC1		
59	CSI0_RSTB				usb1 VSTATUS2
62	DISP0_DAT0		DEBUG_CORE_RUN	EMI_DEBUG5	usb2 TXREADY
63	GPIO_0(CLK0)	EPITO	SRTC_ALARM_DEB	USBH1_PWR	csu TD
64	DISP0_DAT1		DEBUG_EVENT_CHAN_SEL	EMI_DEBUG6	usb2 RXVALID
66	DISP0_DAT2		DEBUG_MODE	EMI_DEBUG7	usb2 RXACTIVE
68	DISP0_DAT3		DEBUG_EVENT_BUS_ERROR	EMI_DEBUG8	usb2 RXERROR
70	DISP0_DAT4		DEBUG_BUS_RWB	EMI_DEBUG9	usb2 SIECLOCK
72	DISP0_DAT5		DEBUG_MATCHED_DMBUS	EMI_DEBUG10	usb2 LINESTATE0
74	DISP0_DAT6		DEBUG_RTBUFFER_WRITE	EMI_DEBUG11	usb2 LINESTATE1
76	DISP0_DAT7		DEBUG_EVENT_CHANNEL0	EMI_DEBUG12	usb2 VBUSVALID
78	DISP0_DAT8		DEBUG_EVENT_CHANNEL1	EMI_DEBUG13	usb2 AVALID

Legend

UART4	AUDMUX4	I2C1	ECSPI2	USBH2
UART5	AUDMUX5	I2C2	CSPI	SPDIF

Table 6-15. Expansion Port Pin-Mux Table (continued)

J78 PIN	J13 Name	i.MX53 Pin Name	ALT(1)	ALT(2)	ALT(3)
79	DISP0_POWER_EN	EIM_D24	GPIO3_24	uart3 TXD_MUX	ecspi1 SS2
80	DISP0_DAT9	DISP0_DAT9	GPIO4_30	pwm2 PWMO	wdog2 WDOG_B
81	DSIP0_SER_nCS	EIM_D20	GPIO3_20	DI0_PIN16	SER_DISP0_CS
82	DISP0_DAT10	DISP0_DAT10	GPIO4_31	USBH2_STP	
84	DISP0_DAT11	DISP0_DAT11	GPIO5_5	USBH2_NXT	
85	DISP0_SER_MISO	EIM_D22	GPIO3_22	DI0_PIN1	DISPB0_SER_DIN
86	DISP0_DAT12	DISP0_DAT12	GPIO5_6	USBH2_CLK	
87	DISP0_SER_MOSI	EIM_D28	GPIO3_28	uart2 CTS	DISPB0_SER_DI0
88	DISP0_DAT13	DISP0_DAT13	GPIO5_7		AUD5_RXFS
89	DISP0_SER_SCLK	EIM_D21	GPIO3_21	DI0_PIN17	DISPB0_SER_CLK
90	DISP0_DAT14	DISP0_DAT14	GPIO5_8		AUD5_RXC
91	DISP0_SER_RS	EIM_D29	GPIO3_29	uart2 RTS	DISPB0_SER_RS
92	DISP0_DAT15	DISP0_DAT15	GPIO5_9	ecspi1 SS1	ecspi2 SS1
94	DISP0_DAT16	DISP0_DAT16	GPIO5_10	ecspi2 MOSI	AUD5_TXC
96	DISP0_DAT17	DISP0_DAT17	GPIO5_11	ecspi2 MISO	AUD5_TXD
98	DISP0_DAT18	DISP0_DAT18	GPIO5_12	ecspi2 SS0	AUD5_TXFS
100	DISP0_DAT19	DISP0_DAT19	GPIO5_13	ecspi2 SCLK	AUD5_RXD
102	DISP0_DAT20	DISP0_DAT20	GPIO5_14	ecspi1 SCLK	AUD4_TXC
104	DISP0_DAT21	DISP0_DAT21	GPIO5_15	ecspi1 MOSI	AUD4_TXD
105	DISP0_nCS0	EIM_D23	GPIO3_23	uart3 CTS	uart1 DCD
106	DISP0_DAT22	DISP0_DAT22	GPIO5_16	ecspi1 MISO	AUD4_TXFS
107	DISP0_nCS1	EIM_A25	GPIO5_2	ecspi2 RDY	DI1_PIN12
108	DISP0_DAT23	DISP0_DAT23	GPIO5_17	ecspi1 SS0	AUD4_RXD
109	DISP0_WR	EIM_D30	GPIO3_30	uart3 CTS	CSI0_D3
110	DISP0_VSYNCH	DI0_PIN3	GPIO4_19	AUD6_TXFS	
112	DISP0_CONTRAST	GPIO_1	GPIO1_1	KEY_ROW5	SSI_EXT2_CLK
114	DISP0_HSYNCH	DI0_PIN2	GPIO4_18	AUD6_TXD	
116	DISP0_DRDY	DI0_PIN15	GPIO4_17	AUD6_TXC	
117	DISP0_RD	EIM_D31	GPIO3_31	uart3 RTS	CSI0_D2

Legend

UART4	AUDMUX4	I2C1	ECSPI2	USBH2
UART5	AUDMUX5	I2C2	CSPI	SPDIF

Table 6-15. Expansion Port Pin-Mux Table (continued)

J78 PIN	J13 Name	ALT(4)	ALT(5)	ALT(6)	ALT(7)
79	DISP0_POWER_EN	cspi SS2	AUD5_RXFS	ecspi2 SS2	uart1 DTR
80	DISP0_DAT9		DEBUG_EVENT_CHANNEL2	EMI_DEBUG14	usb2 VSTATUS0
81	DSIP0_SER_nCS	cspi SS0	EPITO	uart1 RTS	USBH2_PWR
82	DISP0_DAT10		DEBUG_EVENT_CHANNEL3	EMI_DEBUG15	usb2 VSTATUS1
84	DISP0_DAT11		DEBUG_EVENT_CHANNEL4	EMI_DEBUG16	usb2 VSTATUS2
85	DISP0_SER_MISO	cspi MISO		USBOTG_PWR	
86	DISP0_DAT12		DEBUG_EVENT_CHANNEL5	EMI_DEBUG17	usb2 VSTATUS3
87	DISP0_SER_MOSI	cspi MOSI	i2c1 SDA	EXT_TRIG	DI0_PIN13
88	DISP0_DAT13		DEBUG_EVT_CHN_LINES0	EMI_DEBUG18	usb2 VSTATUS4
89	DISP0_SER_SCLK	cspi SCLK	i2c1 SCL	USBOTG_OC	
90	DISP0_DAT14		DEBUG_EVT_CHN_LINES1	EMI_DEBUG19	usb2 VSTATUS5
91	DISP0_SER_RS	cspi SS0	DI0_PIN15	CSI1_VSYNCH	DI0_PIN14
92	DISP0_DAT15		DEBUG_EVT_CHN_LINES2	EMI_DEBUG20	usb2 VSTATUS6
94	DISP0_DAT16	SDMA_EXT_EVENT0	DEBUG_EVT_CHN_LINES3	EMI_DEBUG21	usb2 VSTATUS7
96	DISP0_DAT17	SDMA_EXT_EVENT1	DEBUG_EVT_CHN_LINES4		
98	DISP0_DAT18	AUD4_RXFS	DEBUG_EVT_CHN_LINES5	EMI_DEBUG23	WEIM_CS2
100	DISP0_DAT19	AUD4_RXC	DEBUG_EVT_CHN_LINES6	EMI_DEBUG24	WEIM_CS3
102	DISP0_DAT20		DEBUG_EVT_CHN_LINES7	EMI_DEBUG25	sata_phy TDI
104	DISP0_DAT21		DEBUG_BUS_DEVICE0	EMI_DEBUG26	sata_phy TDO
105	DISP0_nCS0	DI0_DO_CS	DI1_PIN2	CSI1_DATA_EN	DI1_PIN14
106	DISP0_DAT22		DEBUG_BUS_DEVICE1	EMI_DEBUG27	sata_phy TCK
107	DISP0_nCS1	cspi SS1		DIO_D1_CS	
108	DISP0_DAT23		DEBUG_BUS_DEVICE2	EMI_DEBUG28	sata_phy TMS
109	DISP0_WR	DI0_PIN11	DISP1_DAT21	USBH1_OC	USBH2_OC
110	DISP0_VSYNCH		DEBUG_CORE_STATE3	EMI_DEBUG3	usb1 IDDIG
112	DISP0_CONTRAST	pwm2 PWMO	wdog2 WDOG_B	esdhc1 CD	src TESTER_ACK
114	DISP0_HSYNCH		DEBUG_CORE_STATE2	EMI_DEBUG2	usb1 ENDSSN
116	DISP0_DRDY		DEBUG_CORE_STATE1	EMI_DEBUG1	usb1 BVALID
117	DISP0_RD	DI0_PIN12	DISP1_DAT20	USBH1_PWR	USBH2_PWR

Legend

UART4	AUDMUX4	I2C1	ECSPI2	USBH2
UART5	AUDMUX5	I2C2	CSPI	SPDIF

Table 6-15. Expansion Port Pin-Mux Table (continued)

7. Board Accessories

7.1. Debug Card

A debug card having a RS-232, a JTAG, and an Ethernet is provided for developer in the board kit. The developer can connect the debug card with the main board to develop the system. **Figure 7-1** shows the debug card available in the MCIMX53SMD board.

The schematics and layout of the debug card can be found on the http://www.freescale.com/imxsabre Web page.

Figure 7-1. Debug Card

8. Mechanical PCB Information

The overall dimensions of the MCIMX53SMD board are shown in **Figure 8-1**.

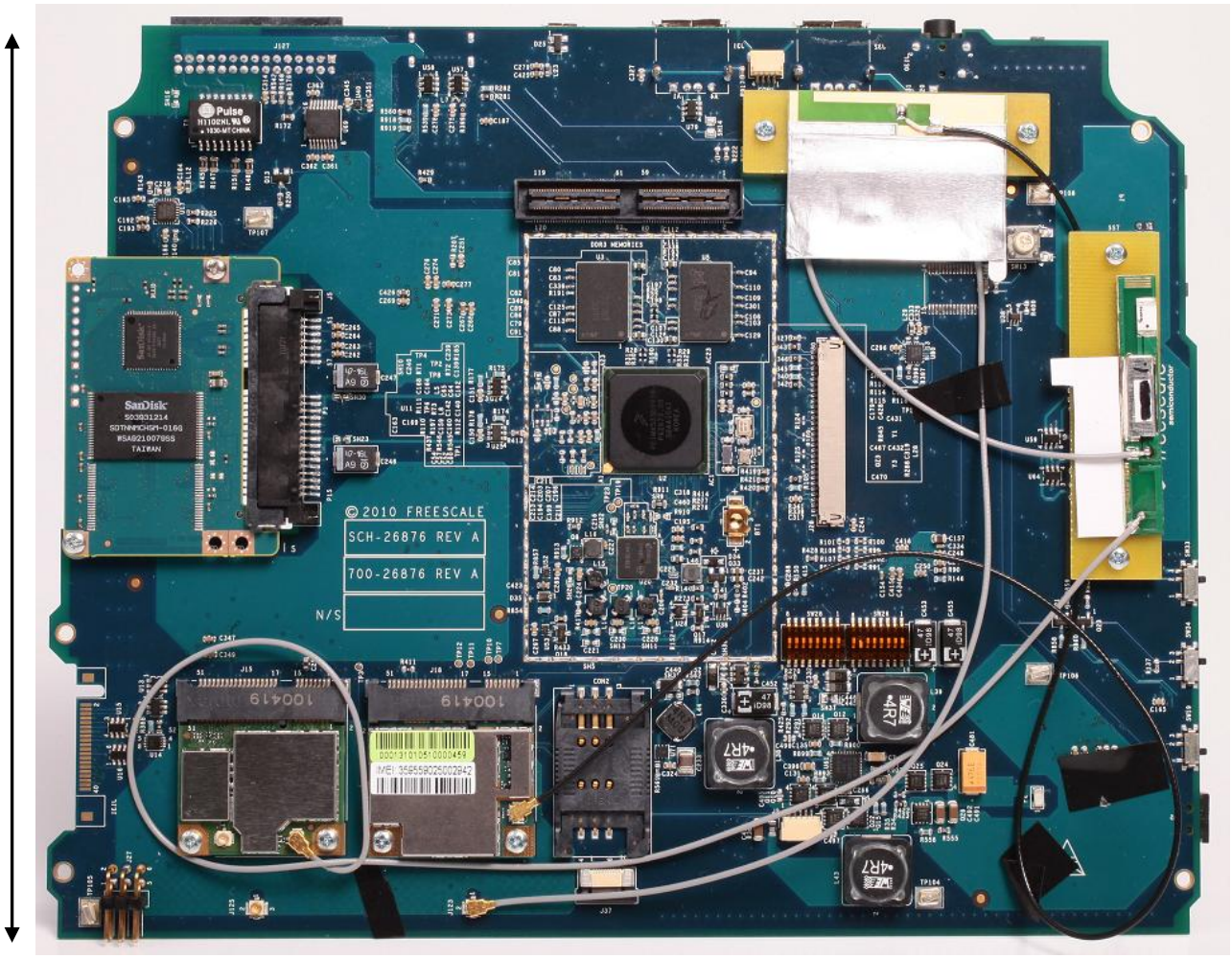


Figure 8-1. MCIMX53SMD Board Dimensions

The MCIMX53SMD board PCB was made by using the standard 8-layer technology. The material used was FR-4 Hi Temp. The board stack up is as follows:

- Top Layer
- Ground-1 Layer
- Signal-1 Layer
- GND/Power-1 Layer
- GND/Power-2 Layer
- Signal-2 Layer
- Ground-2 Layer
- Bottom Layer

The stack up information provided by the PCB Fabrication Facility is as shown in **Table 8-1.** Widths and thickness are shown in mils (1 mils equals to 0.0254 millimeters). Impedances are shown inΩ. The material used in calculating this stack up was 370HR.

				Single End Trace				Differential Pair Traces					
Layer	Thickness	Description	Copper Oz.	Trace Width	Calculated Impedance	Target Impedance	Reference Plane	Trace Width	Space Width	Diff Pairs (Pitch)	Calculated Impedance	Target Impedance	Reference Plane
	0.70	Mask											
	1.20	Plating											
1	0.60	Signal	0.50	8.50	50.32	50	2	4.75	5.25	10	100.82	100	2
				3.25	73.94	75	2	6.25	4.75	11	89.51	90	2
	5.00	Prepreg											
2	0.60	GND	0.50										
	4.00	Core											
3	0.44	Signal	0.37					3.75	6.25	10	89.69	90	2,4
				3.25	49.60	50	2,4	3.00	6.00	9	99.88	100	2,4
	3.00	Prepreg											
4	0.60	Power	0.50										
	30.00	Core											
5	0.60	Power	0.50										
	3.00	Prepreg											
6	0.44	Signal	0.37					3.75	6.25	10	89.69	90	5,7
				3.25	49.60	50	5,7	3.00	6.00	9	99.88	100	5,7
	4.00	Core											
7	0.60	GND	0.50										
	5.00	Prepreg											
8	0.60	Signal	0.50	8.50	50.32	50	7	4.75	5.25	10	100.82	100	7
				3.25	73.94	75	7	6.25	4.75	11	89.51	90	7
	1.20	Plating											
	0.70	Mask											
	62.28	=	Total Thickness										

Table 8-1. Board Stack Up Information

9. Board Verification

The On Board Diagnostic Scan (OBDS) tool used by the factory acceptance test tools can be downloaded from the http://www.freescale.com/imxsabre Web page.

To access the OBDS tool, a serial cable and a host PC running a terminal program (such as, TerraTerminal or HyperTerminal) will be required. After connecting the host terminal to the MCIMX53SMD board, press the power button on the board. Before U-BOOT completes the Autoboot countdown (within 3 seconds of pressing the power button), press any key on the host computer. This will stop the Ubuntu Kernel from continuing the boot process and allow the developer to access the code on the SD card. On the host computer terminal window, type the following two lines:

mmc read 0 708000 200 3e5

go 70800000

This will begin the OBDS diagnostic tool. The tool has 15 tests that it can perform. They are as follows:

1. MAC Address confirmation
2. Debug UART Test
3. DDR3 Test
4. USBH1 Enumeration Test (Upper Host Port)
5. Secure Real Time Clock Test
6. Dialog PMIC ID Test
7. SATA Test
8. I2C Device Test
9. GPIO Test
10. Ethernet Test
11. I2S Audio Test
12. LVDS Display Test
13. VGA Video Test
14. HDMI Daughter Card Test
15. MMC/SD Card Test

The tests are straight forward, and if a supporting piece of equipment is required, the test will prompt you for it. In order to complete all the tests, you would need to have the following equipments:

- SATA Test: Attached SATA device required.
- Ethernet Test: The Ethernet loopback test plug as described below is required.
- Headphone Test: A set of earphones or speakers are required.
- LVDS Test: The optional LVDS display kit is required.
- VGA Video Test: Connection to a VGA monitor is required.
- HDMI Test: The optional HDMI card is required.
- MMC/SD Card Test: A full-size SD card is required in card slot J5.

If the developer does not have one or more of the above items, the test can easily be skipped when asked if the user would like to perform the test. A complete cycle of tests covers 16 different aspects of the board. When the last test is run, the OBDS tool will print out a summary of the test results. A failure in any one particular area would indicate that there is a hardware fault with the MCIMX53SMD board that should be addressed. If the developer code does not function correctly even after successfully performing all the tests, the problem is most likely with the code. A more detailed description of the tests is as follows:

1) **MAC Address confirmation:** The i.MX53 processor reads the MAC address programmed into the processor eFUSEs and prints it out on the terminal window. The outputted address should match the MAC address label on the MCIMX53SMD board. If they match, the test was successful.

2) **UART Test:** When the test is running, the test expects different characters to be inputted from the keyboard of the host computer. When a character is inputted, the i.MX53 processor takes the character and transmits it to the terminal window, and then asks the user to verify if the character is correct by pressing the ‘y’ key. The user can exit the test by pressing the ‘x’ key.

3) **DDR Test:** The test writes predetermined data onto the DDR3 memory, reads those memory blocks back out, and then compares the two values for errors. If the values match, the test was successful.

4) **USBH1 Enumeration Test:** Any USB device is plugged into the upper HOST connector (the lower port is connected to the USBOTG module). After confirming that a USB device is plugged in, the i.MX53 processor will read the device enumeration data and print it out on the terminal window. If the processor cannot read the enumeration information, the test has failed.

5) **Secure Real Time Clock Test:** The i.MX53 processor checks to make sure the RTC clock is counting. If the clock is counting, the test passes.

6) **PMIC Device ID Test:** The i.MX53 processor attempts to communicate with the PMIC using the attached I2C channel. If the two devices communicate, the test passes.

7) **SATA Test:** The processor attempts to communicate with an attached SATA device. If the processor detects the internal 50 MHz clock signal and is able to communicate with the attached SATA device, the test passes.

8) **I2C Test:** The processor attempts to communicate with one of the I2C devices on the MCIMX53SMD board. If communications is done successfully, the test passes.

9) **GPIO Test:** The processor drives the USER LED light controlled by PATA_DA_1 (pin L3) alternately to high and low. If the user light is blinking, the test passes.

10) **FEC Ethernet Test:** The processor drives a data packet out of the Ethernet Jack into the loopback cable, and then receives the test packet back. If the received packet matches the sent packet, the test passes.

11) **I2S Audio Test:** The processor gives a tone to the Audio CODEC. If the tone can be heard through both speakers of the attached headphones, the test passes. After the user requests the test to be run, the user is prompted to insert a headphone set into jack (J18). When the headphones are connected, the user presses the ‘y’ key to confirm the headphones are attached. A sound is played. The test will then prompt you to replay the tone if needed. If the tone is no longer needed, the test will ask the user if the tone was heard.

12) **LVDS Display Test:** If this test is selected, an image will be displayed on the attached LVDS panel. Once the image is displayed, the test will prompt the user to confirm whether or not the image is seen. If the image is seen, the test passes.

13) **VGA Video Test:** If this test is selected, a video will be displayed on the attached video monitor. Once the video is displayed, the test will prompt the user to confirm whether or not the video is seen. If the video is seen, the test passes.

14) **HDMI Test:** If this test is selected, an image will be displayed on the attached video monitor. Once the image is displayed, the test will prompt the user to confirm whether or not the image is seen. If the image is seen, the test passes.

15) **MMC/SD Card Test:** If the user selects this test to be run, the user will be prompted to insert an MMC/SD card into the full-size SD card slot (J5). When the user confirms that the card is present, the processor will attempt to read the current SD card settings and manufacturing information on the SD card. If the processor can read this information, the test passes.

The only special equipment required to complete the bank of OBDS tests is the Ethernet loopback cable. This can be purchased online (single plug Ethernet Lookback Cable) or it can be created by the developer by cutting one end of an unneeded Ethernet cable and connecting pin 1 wire to pin 3 wire, and connecting pin 2 wire to pin 6 wire. All other wires remain unconnected. The four wires used will be solid Green, solid Orange, Green/White stripe, and Orange/White stripe. The solid colors are connected together and the striped colors are connected together. While the solid colors will always be connected to pins 2 and 6, the specific pin a color is attached to depends on the plug used. They same is true for the striped wires connected to pins 1 and 3. **Figure 9-1** shows a diagram of an Ethernet loopback cable.

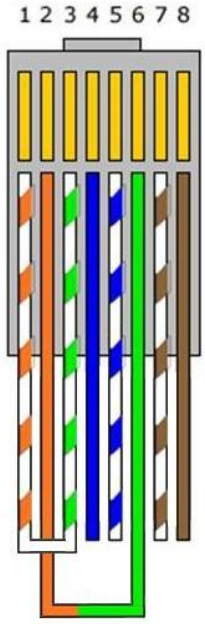


Figure 9-1. Ethernet Loopback Cable

10. Troubleshooting

The MCIMX53SMD board does not have specific troubleshooting features designed into the board. The board has proven robust during the initial test and development periods and should provide years of good service to the developer if treated with due caution. The test pads that are included on the schematic and on the board were not specifically designed for testing, but were placed on the board for developers who wanted to make wire connections to specific pins that might not be available without the test pads. One basic troubleshooting technique available to developers is to measure the voltage rail outputs on all the rails coming from the PMIC. The subsection on PMIC voltage rails presents a diagram with points that can be used by the developer take measurements. A second basic troubleshooting technique would be to measure the clock frequencies to ensure that the clock is running correctly. The crystals and oscillators are located in the design section under the i.MX53 processor.

Aside from actual hardware difficulties, **Table 10-1** presents some other issues that may help the developer solve technical difficulties:

Symptoms	Possible Problem	Action
No 15V power to the	Attached power supply is not	Use the power supply that came

MCIMX53SMD board, no RED LED light.	within the 14.5V – 15.5V range.	with the MCIMX53SMD board kit.
	F2 fuse has blown.	Use a multimeter to check whether the part is open. If yes, replace the fuse with a new 3A, 0603 surface mount fuse.
No debug information on the host Computer terminal window.	Incorrect serial cable used (for example, null modem cable)	Verify that serial cable is correct.

Table 10-1. Problem Resolution Table

10.1. PMIC Voltage Rail Test Points

To assist the developer in determining whether the PMIC voltage rails are outputting the correct voltage levels, **Figures 10-1** shows the output capacitor on each regulator output, with the ground pin colored yellow and the power pin colored red. **Tables 10-1** shows the expected voltage value for each capacitor.

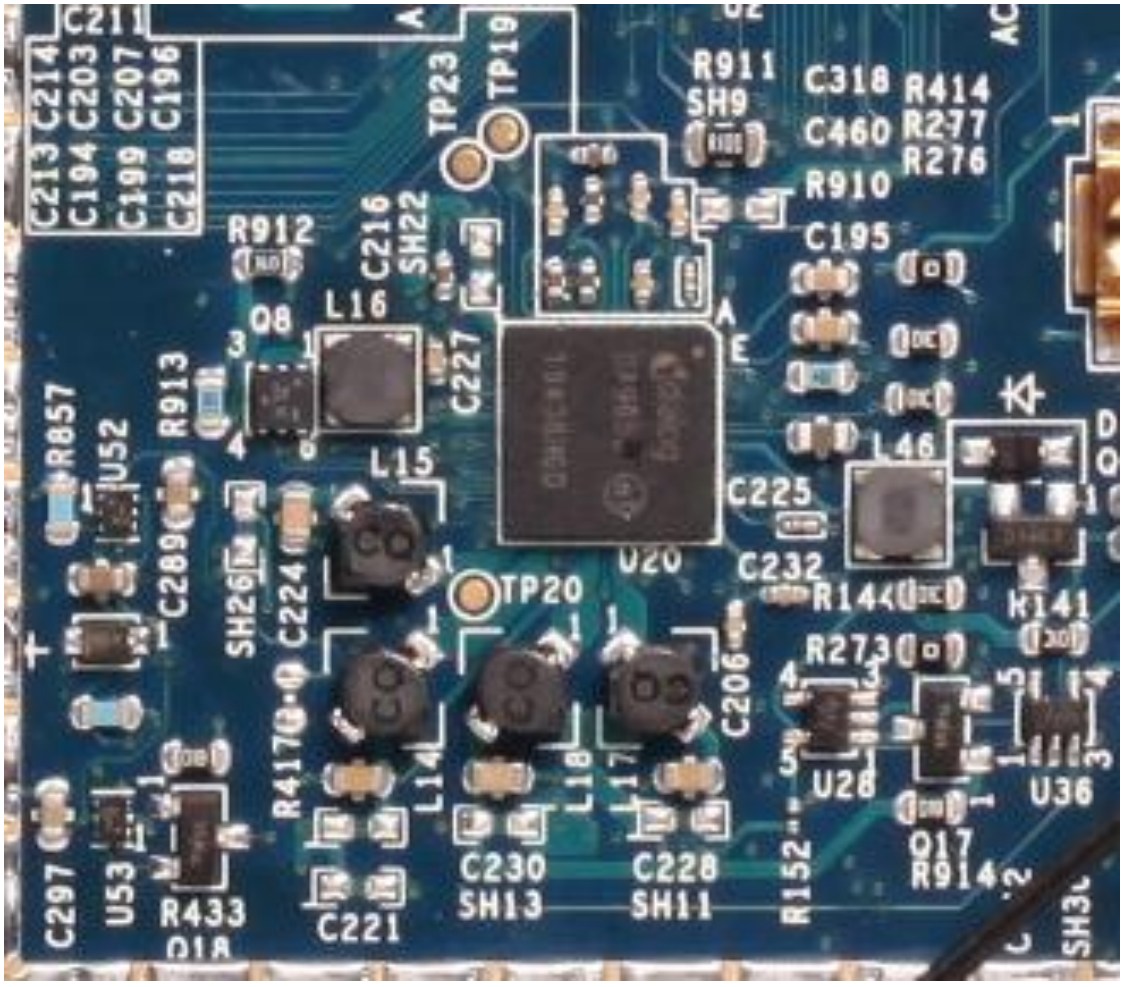


Figure 10-1. Regulator Output Capacitor Positions Top

Capacitor	Regulator	Value
C199	VLDO2	1.3V
C214	VLDO9	1.5V
C216	VLDO10	1.3V
C213	VLDO8	1.8V
C211	VLDO7	2.75V
C194	VLDO3	3.3V
C203	VLDO4	2.775V
C210	VLDO6	1.3V
C207	VLDO5	1.3V
C196	VLDO1	1.3V
C218	VDDCORE	2.5V
C221	VBUCKPERI	2.5V
C224	VBUCKMEM	1.5V
C230	VBUCKPRO	1.3V
C228	VBUCKCORE	1.1V

Table 10-2. Output Capacitors and Values Top

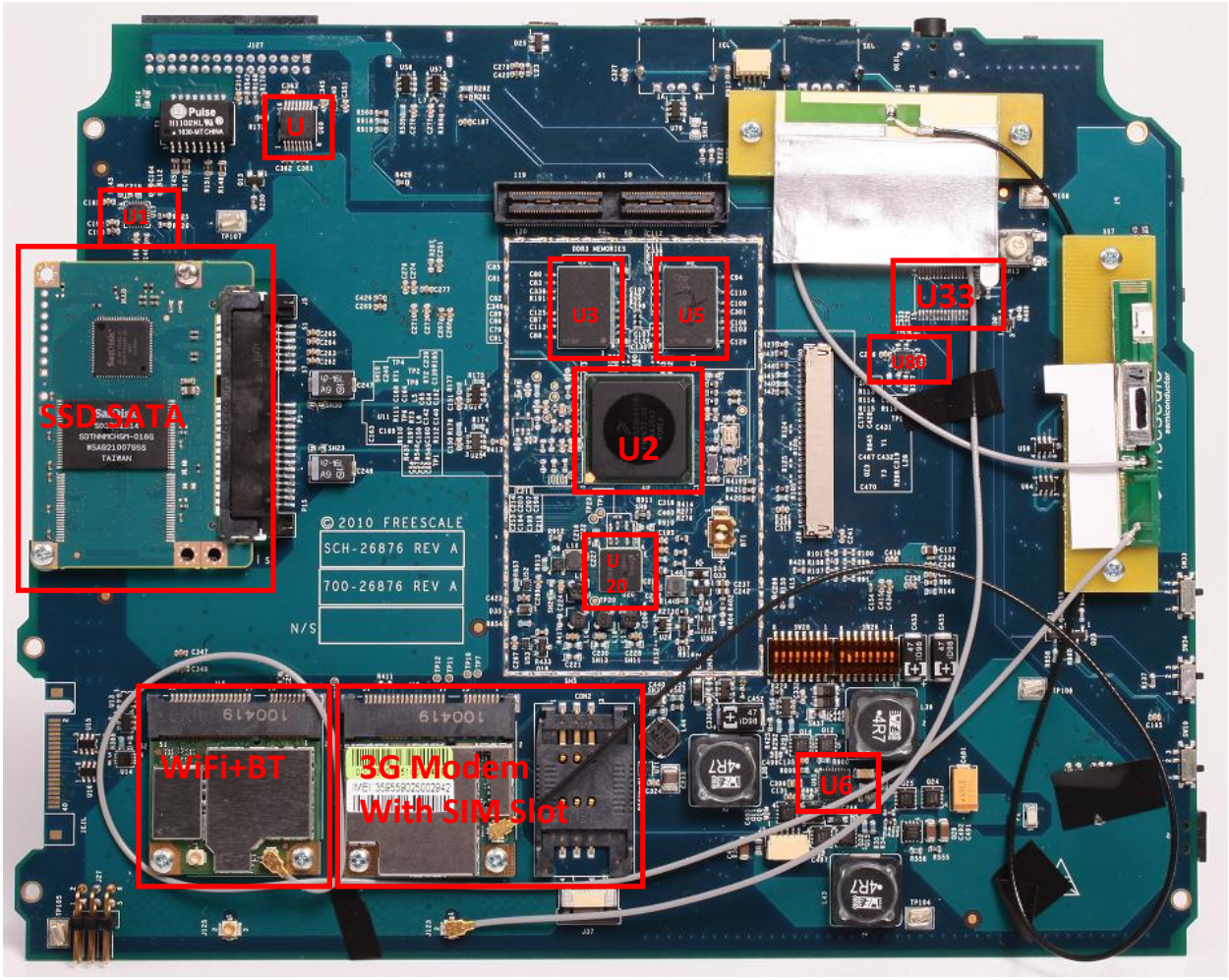
11. PCB Component Locations

To help the developer in locating the major components on the MCIMX53SMD board, locations of the components have been highlighted and annotated in the following figures:

Figure 11-1. Major Component Highlights Top
Figure 11-2. Major Component Highlights Bottom

The assembly drawings for all component locations are available for easy reference while working on the MCIMX53SMD board. Graphical representations of the assembly drawings are shown in the following figures:

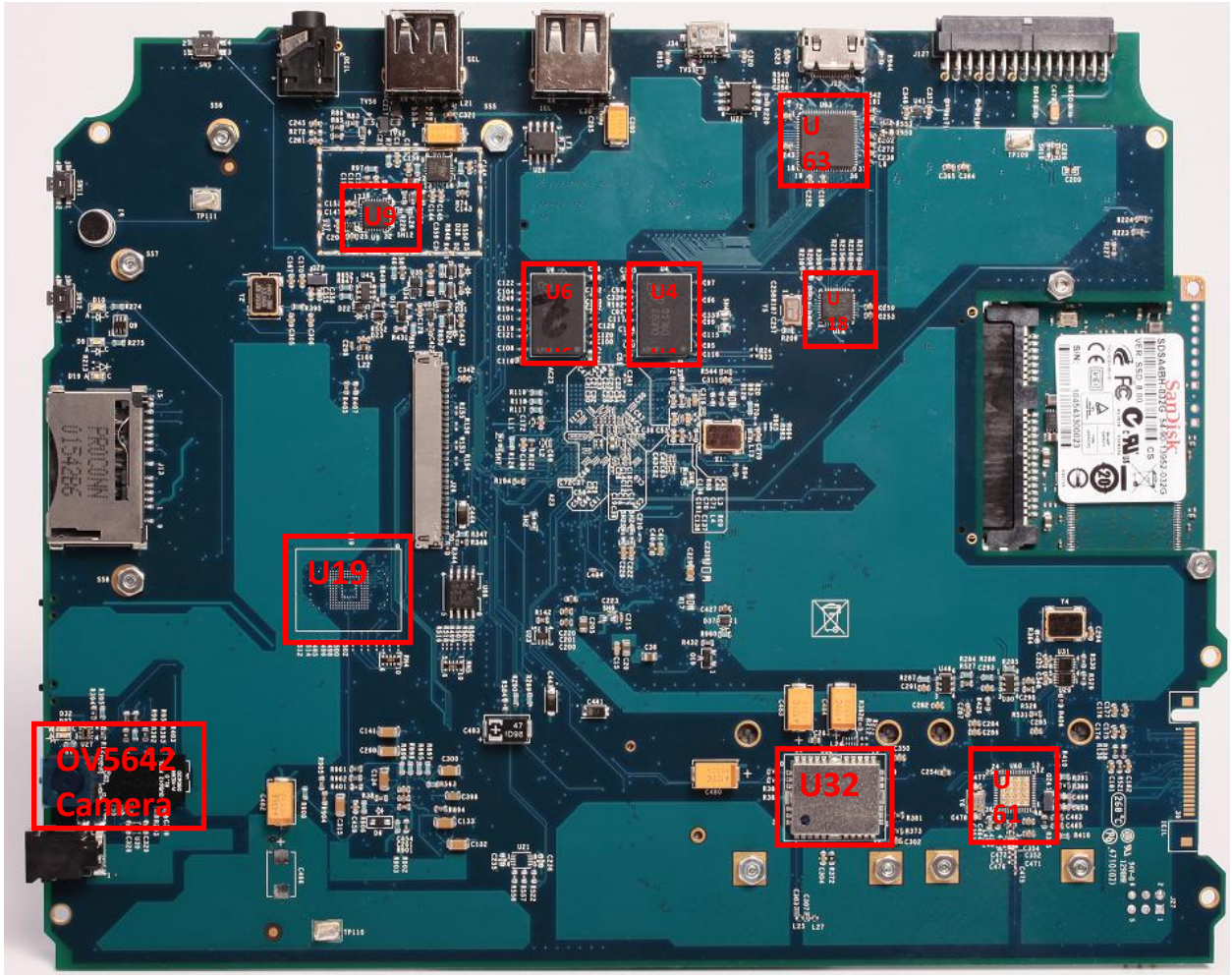
Figure 11-3. Assembly Drawing Top
Figure 11-4. Assembly Drawing Bottom



U2	i.MX53 Application Processor
U3	DDR3 SDRAM
U5	DDR3 SDRAM
U17	LAN8720 FEC
U33	AT97SC3203S TPM (DNP)

U20	Dialog DA9053 PMIC
U80	MMA8452QT Accelerometer
U24	RS232 UART Transceiver
U61	MAX17085B DCDC&Charger

Figure 11-1. Major Component Highlights Top



U9	SGTL5000 Audio Codec
U4	DDR3 SDRAM
U6	DDR3 SDRAM
U19	eMMC

U63	SiI9022 HDMI
U18	USB2514 USB 1-to-4
U32	GM22 GPS Module
U60	MC1323X ZigBee

Figure 11-2. Major Component Highlights Bottom

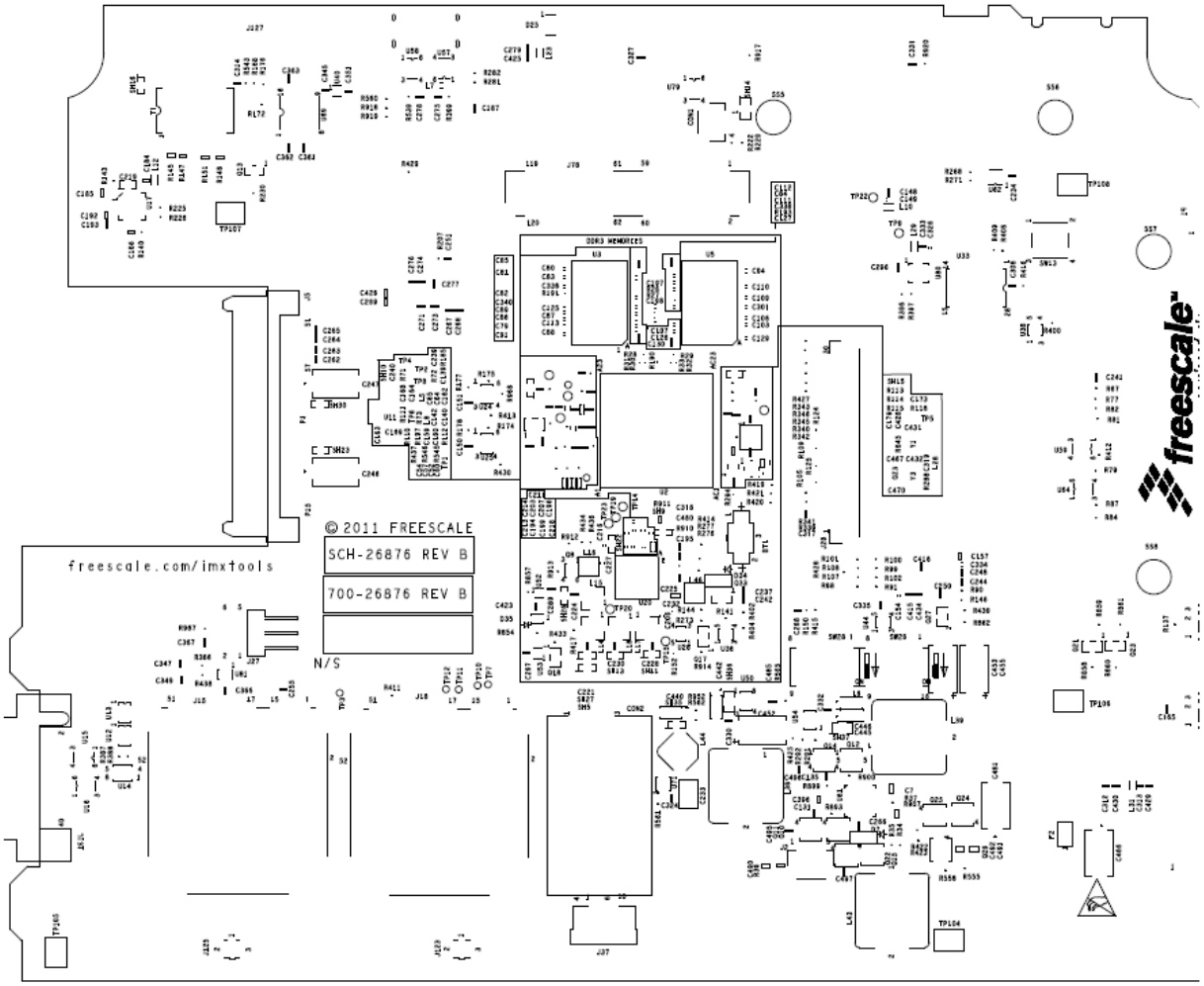


Figure 11-3. Assembly Drawing Top

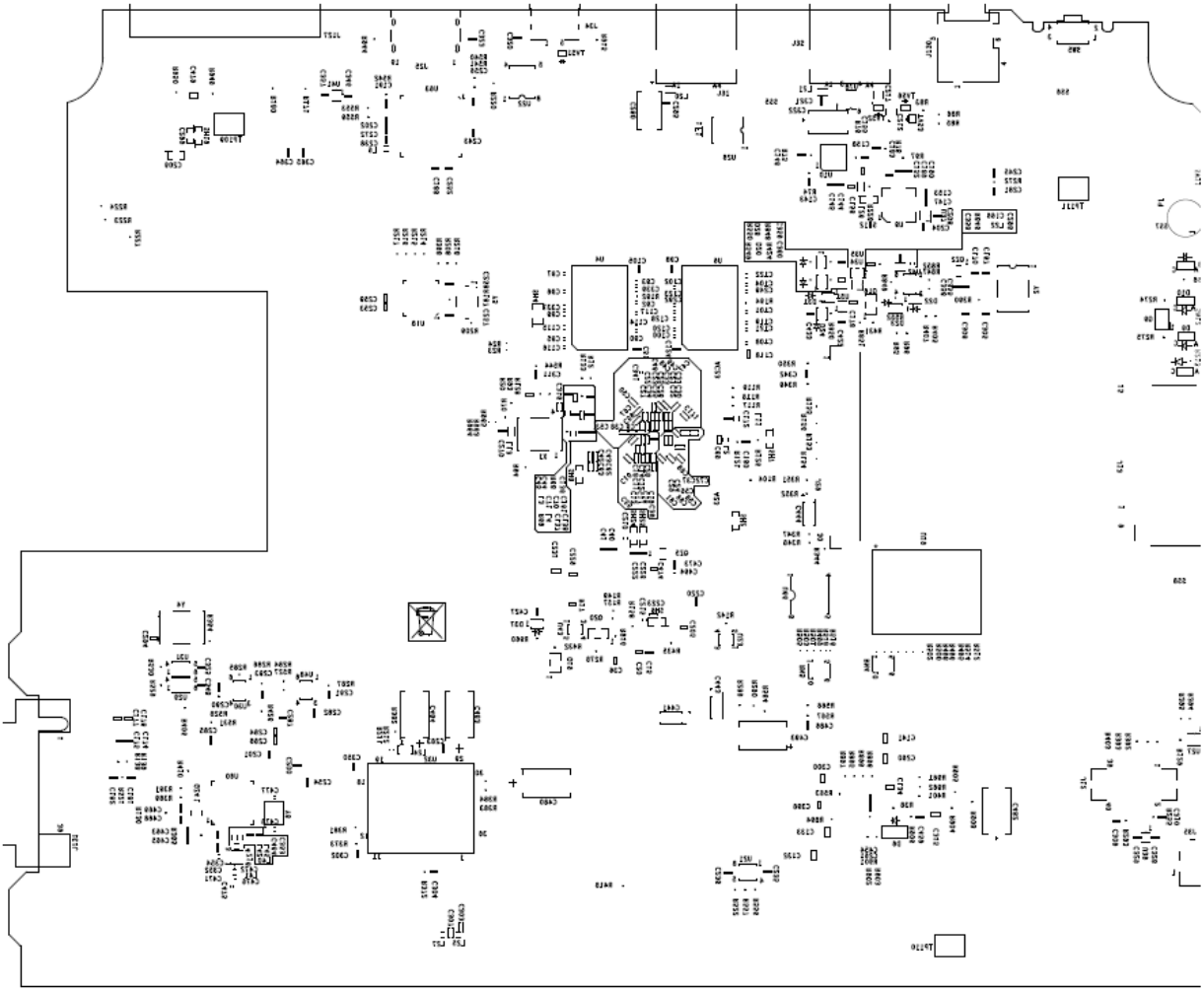


Figure 11-4. Assembly Drawing Bottom

12. Schematics

The schematics consist of 22 pages. The schematic pages can be downloaded from the following Web page:

http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=RDIMX53SABRETAB&fpsp=1&tab=Design_Tools_Tab

13. Bill of Materials

The Bill of Materials (BOM) used to manufacture the MCIMX53SMD board is presented in this section. The capacitors and resistors used are considered as generic type components and do not include manufacturer names or part numbers. The remaining parts have manufactures and part numbers provided for the primary part specified. Second source vendors are not included. The final section of the BOM includes the list of parts that are not populated on the MCIMX53SMD board at the time of manufacturing. The BOM for MCIMX53SMD board can be downloaded from the following Web page:

http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=RDIMX53SABRETAB&fpsp=1&tab=Design_Tools_Tab

14. FCC Statement

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense.

Modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment under FCC rules.