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MAXIM

Full-Bridge Controller for Piezoelectric Transformers

MAX8785A

General Description

Liquid-crystal display (LCD) enclosures and cold-cathode fluorescent lamps (CCFL) used in notebook computer and portable electronic displays are becoming increasingly narrow, generating the need for a low-profile CCFL power supply. Recent advances in piezoelectric transformers (PZTs) have made it possible to develop smaller, more efficient, and safer backlight inverters for portable displays. Piezoelectric transformers have shown better performance than magnetic transformers with respect to efficiency, EMI requirements, human safety, and form factor. The MAX8785A is a full-bridge CCFL controller for piezoelectric transformer-based backlight power supplies. The full-bridge topology provides a high-spectral purity sinusoidal drive that helps the PZT convert electrical energy to mechanical and back to electrical energy efficiently.

The MAX8785A employs a feed-forward control architecture that provides excellent line-and-load regulation while maintaining relatively constant switching frequency. The MAX8785A provides protection against open-lamp, secondary short-circuit, lamp arcing, and secondary overvoltage with adjustable timeout periods.

The MAX8785A guarantees lamp striking by sweeping the switching frequency from high to low until the lamp is struck. The MAX8785A achieves 10:1 dimming range using a digital pulse-width modulation (DPWM) method. CCFL brightness can be set with an analog voltage on the CNTL pin or through an external signal at LSYNC. The maximum switching frequency and DPWM frequency can be adjusted with external resistors.

The MAX8785A gate drivers can drive large power MOSFETs typically used in high-power CCFL applications. An internal 5.35V linear regulator powers the MOSFET drivers and most of the internal circuitry. The MAX8785A is available in a low-profile, 28-pin thin QFN package and operates over the -40°C to +85°C temperature range.

Applications

Notebook LCDs

LCD TVs and Monitors

Simplified Operating Circuit appears at end of data sheet.

Features

♦ **Resonant, All n-Channel, Full-Bridge Topology**
♦ **Wide Input-Voltage Range (4.5V to 28V)**
♦ **Frequency Sweeping Guarantees CCFL Striking**
♦ **Feed-Forward Control Provides Excellent Line-Transient Response**
♦ **Programmable Maximum Switching Frequency**
♦ **Analog or Digital DPWM**
♦ **Lamp-Out Detection with Adjustable Timeout**
♦ **Fault Protection with Adjustable Timeout**
♦ **Primary Current Limit with $R_{DS(ON)}$ Sensing**
♦ **Strong Gate Drivers Support Large External MOSFETs**
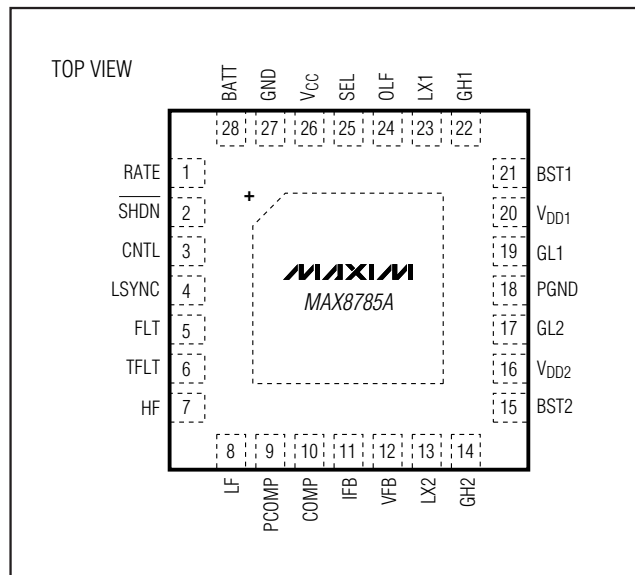♦ **28-Pin Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8785AETI+	-40°C to +85°C	28 Thin QFN*

+Denotes lead-free package.
*EP = Exposed pad.

Pin Configuration

Maxim Integrated Products **1**

Full-Bridge Controller for Piezoelectric Transformers

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ABSOLUTE MAXIMUM RATINGS

BATT, RATE, LX1, LX2 to GND ....-0.3V to +30V
BST1, BST2 to GND ....-0.3V to +36V
BST1 to V_{DD1}, BST2 to V_{DD2}...................................-0.3V to +30V
BST1 to LX1...-0.3V to +6V
BST2 to LX2...-0.3V to +6V
V_{CC}, V_{DD1}, V_{DD2}, CNTL, LSYNC, $\overline{SHDN}$,
 FLT to GND..-0.3V to +6V
GH1 to LX...-0.3V to (VBST1 + 0.3V)
GH2 to LX2...-0.3V to (VBST2 + 0.3V)
GL1 to GND ....-0.3V to (V_{DD1} + 0.3V)
GL2 to GND ....-0.3V to (V_{DD2} + 0.3V)

COMP, HF, LF, PCOMP, SEL,
 TFLT to GND...-0.3V to (V_{CC} + 0.3V)
IFB, VFB, OLF to GND...-6V to +6V
PGND to GND ....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
 28-Pin Thin QFN (derate 21.3mW/°C above +70°C)...1702.1mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{BATT} = 12V, V_{DD1} = V_{DD2} = $V_{\overline{SHDN}}$ = 5.35V, R_{RATE} = 190kΩ, **T_A = 0°C to +85°C**, unless otherwise noted. See Figure 1. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BATT Input Voltage Range	V_{CC} = V_{DD1} = V_{DD2} = open	5.5		28.0	V
	V_{CC} = V_{DD1} = V_{DD2} = BATT	4.5		5.5	
BATT Quiescent Current	V_{BATT} = 28V		1.5	6	mA
BATT Quiescent Current, Shutdown	$V_{\overline{SHDN}}$ = 0, V_{BATT} = 28V		10	25	µA
V_{CC} Output Voltage, Normal Operation	6V < V_{BATT} < 28V, 0 < I_{LOAD} < 20mA	5.20	5.35	5.50	V
V_{CC} Output Voltage, Shutdown	$V_{\overline{SHDN}}$ = 0, no load	3.5	4.6	5.5	V
V_{CC} Undervoltage-Lockout Threshold	V_{CC} rising (leaving lockout)			4.5	V
	V_{CC} falling (entering lockout)	4.0			
V_{CC} Undervoltage-Lockout Hysteresis			150		mV
GH1, GH2, GL1, and GL2 On-Resistance, Low State	I_{TEST} = 10mA		1	3	Ω
GH1, GH2, GL1, and GL2 On-Resistance, High State	I_{TEST} = 10mA		4	8	Ω
BST1, BST2 Leakage Current	V_{BST1} = 24V, V_{LX1} = 19V; V_{BST2} = 24V, V_{LX2} = 19V, V_{BATT} = 28V			5	µA
LX1, LX2 Leakage Current	V_{BATT} = 28V			5	µA
Minimum On-Time		240	370	500	ns
Duty Cycle	V_{BATT} = 8V, R_{RATE} = 190kΩ, R_{HF} = 100kΩ	22	25	28	%
	V_{BATT} = 16V, R_{RATE} = 190kΩ, R_{HF} = 100kΩ	10.8	12.50	14.2	
	V_{BATT} = 24V, R_{RATE} = 190kΩ, R_{HF} = 100kΩ	7.5	8.5	9.5	
	V_{BATT} = 12V, R_{RATE} = 150kΩ, R_{HF} = 100kΩ		14		
	V_{BATT} = 12V, R_{RATE} = 300kΩ, R_{HF} = 100kΩ		25		
Maximum Duty Cycle				45	%
Current-Limit Threshold	LX1 - PGND, LX2 - PGND	370	400	430	mV
Current-Limit Leading-Edge Blanking		240	370	500	ns
IFB Regulation Point		760	800	840	mV
IFB Input Bias Current	0 < V_{IFB} < +3V	-2		+2	µA
	-3V < V_{IFB} < 0	-225			

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ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = 12V, V_{DD1} = V_{DD2} = $V_{\overline{SHDN}}$ = 5.35V, R_{RATE} = 190kΩ, **T_A = 0°C to +85°C**, unless otherwise noted. See Figure 1. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IFB Lamp-Out Threshold	Reject 1µs glitches	720	800	880	mV
IFB-to-COMP Transconductance	1V < V_{COMP} < 3V	50	100	150	µs
COMP Output Impedance			10		MΩ
COMP Maximum Voltage Threshold		3.15	3.25	3.35	V
COMP Discharge Current During Overvoltage	V_{IFB} = 800mV, V_{VFB} = 2.5V, V_{COMP} = 2V	0.5	1.0	2.0	mA
Initial Startup COMP Charging Current		7	9	11	µA
PCOMP Impedance			1		MΩ
VFB Input Bias Current	-4V < V_{VFB} < +4V	-2		+2	µA
VFB Overvoltage Threshold	V_{FB} rising	2.05	2.25	2.45	V
VFB Short-Circuit Threshold	V_{FB} rising	200	230	260	mV
OLF Input Bias Current	-4V < V_{OLF} < +4V	-2		+2	µA
OLF Trip Threshold	OLF rising	1.1	1.2	1.3	V
Main Oscillator Frequency	R_{HF} = 100kΩ, V_{COMP} = 0.0V	58.0	60.0	62.0	kHz
	R_{HF} = 100kΩ, V_{COMP} = 3.0V		50		
	R_{HF} = 150kΩ, V_{COMP} = 0.0V		40.0		
	R_{HF} = 150kΩ, V_{COMP} = 3.0V		33.3		
	R_{HF} = 75kΩ, V_{COMP} = 0.0V		80.0		
	R_{HF} = 75kΩ, V_{COMP} = 3.0V		66.6		
DPWM Chopping Frequency	R_{LF} = 150kΩ	202	208	214	Hz
	R_{LF} = 103kΩ		300		
	R_{LF} = 315kΩ		100		
DPWM Dimming Resolution	Guaranteed monotonic		8		Bits
CNTL Minimum Duty-Cycle Threshold		0.20	0.23	0.26	V
CNTL Maximum Duty-Cycle Threshold		1.9	2.0	2.1	V
CNTL Input Current	0 < V_{CNTL} < 2.0V	-0.1		+0.1	µA
LSYNC Input Low Voltage				0.8	V
LSYNC Input High Voltage		2.1			V
LSYNC Input Hysteresis			200		mV
LSYNC Input Bias Current	0 < V_{LSYNC} < 5.5V	-1		+1	µA
LSYNC Input Frequency Range	R_{LF} = 150kΩ	120		280	Hz
LSYNC Minimum Duty Cycle		10			%
SEL Input Low Voltage				0.8	V
SEL Input High Voltage		2.1			V
SEL Input Hysteresis			200		mV
SEL Input Bias Current	0 < V_{SEL} < 5.5V	-1		+1	µA
$\overline{SHDN}$ Input Low Voltage				0.8	V
$\overline{SHDN}$ Input High Voltage		2.1			V
$\overline{SHDN}$ Input Hysteresis			100		mV

Full-Bridge Controller for Piezoelectric Transformers

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = 12V, V_{DD1} = V_{DD2} = $V_{\overline{SHDN}}$ = 5.35V, R_{RATE} = 190kΩ, **T_A = 0°C to +85°C**, unless otherwise noted. See Figure 1. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Input Bias Current	0 < $V_{\overline{SHDN}}$ < 5.5V	-1		+1	µA
TFLT Charging Current	V_{VFB} > 2.4V or V_{IFB} < 720mV; V_{OLF} < 1.1V; V_{TFLT} = 2.0V	0.60	0.75	0.90	µA
	V_{VFB} < 2.05V and V_{IFB} > 880mV; V_{OLF} < 1.1V; V_{TFLT} = 2.0V	-1	-0.75	-0.5	
	V_{VFB} < 200mV or V_{OLF} > 1.3V; V_{TFLT} = 2.0V	2.24	2.8	3.36	mA
TFLT Trip Threshold	TFLT rising	2.90	3.0	3.10	V
TFLT Sink Current	V_{TFLT} = 2.0V	80	135	160	mA
FLT Sink Current	V_{TFLT} = 3.1V, V_{FLT} = 0.4V	1			mA
FLT Leakage Current	V_{TFLT} = 0, V_{FLT} = 5.5V			1	µA

ELECTRICAL CHARACTERISTICS

(V_{BATT} = 12V, V_{DD1} = V_{DD2} = $V_{\overline{SHDN}}$, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BATT Input Voltage Range	V_{CC} = V_{DD1} = V_{DD2} = open	5.5		28.0	V
	V_{CC} = V_{DD1} = V_{DD2} = BATT	4.5		5.5	
BATT Quiescent Current	$V_{\overline{SHDN}}$ = 5.5V, V_{BATT} = 28V			6	mA
BATT Quiescent Current, Shutdown	$V_{\overline{SHDN}}$ = 0			25	µA
V_{CC} Output Voltage, Normal Operation	$V_{\overline{SHDN}}$ = 5.5V, 6V < V_{BATT} < 28V, 0 < I_{LOAD} < 20mA	5.20		5.50	V
V_{CC} Output Voltage, Shutdown	$V_{\overline{SHDN}}$ = 0, no load	3.5		5.5	V
V_{CC} Undervoltage-Lockout Threshold	V_{CC} rising (leaving lockout)			4.5	V
	V_{CC} falling (entering lockout)	3.95			
GH1, GH2, GL1, and GL2 On-Resistance, Low State	I_{TEST} = 10mA			3	Ω
GH1, GH2, GL1, and GL2 On-Resistance, High State	I_{TEST} = 10mA			8	Ω
BST1, BST2 Leakage Current	V_{BST1} = 24V, V_{LX1} = 19V; V_{BST2} = 24V, V_{LX2} = 19V; V_{BATT} = 28V			5	µA
LX1, LX2 Leakage Current	V_{BATT} = 28V			5	µA
Minimum On-Time			210	420	ns
Duty Cycle	V_{BATT} = 8V, R_{RATE} = 190kΩ, R_{HF} = 100kΩ	22		28	%
	V_{BATT} = 16V, R_{RATE} = 190kΩ, R_{HF} = 100kΩ	10.8		14.2	
	V_{BATT} = 24V, R_{RATE} = 190kΩ, R_{HF} = 100kΩ	7.50		9.50	
Maximum Duty Cycle				45	%
Current-Limit Threshold	LX1 - PGND, LX2 - PGND	370		430	mV

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ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = 12V, V_{DD1} = V_{DD2} = $V_{\overline{SHDN}}$, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

| PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Leading-Edge Blanking		240		500	ns
IFB Regulation Point		760		840	mV
IFB Input Bias Current	$0 < V_{IFB} < +3V$	-2		+2	μA
	$-3V < V_{IFB} < 0$	-225			
IFB Lamp-Out Threshold	Reject 1μs glitches	720		880	mV
IFB-to-COMP Transconductance	$1V < V_{COMP} < 3V$	50		150	μs
COMP Discharge Current During Overvoltage	V_{IFB} = 800mV, V_{VFB} = 2.5V, V_{COMP} = 2V	0.5		2.0	mA
Initial Startup COMP Charging Current		7		11	μA
COMP Maximum Voltage Threshold		3.15		3.35	V
VFB Input Bias Current	$-4V < V_{VFB} < +4V$	-2		+2	μA
VFB Overvoltage Threshold	V_{FB} rising	2.05		2.45	V
VFB Short-Circuit Threshold	V_{FB} rising	200		260	mV
OLF Input Voltage Range		-4		+4	V
OLF Input Bias Current	$-4V < V_{OLF} < +4V$	-2		+2	μA
OLF Trip Threshold	OLF rising	1.1		1.3	V
Main Oscillator Frequency	R_{HF} = 100kΩ, V_{COMP} = 0V	57		63	kHz
DPWM Chopping Frequency	R_{LF} = 150kΩ	198		218	Hz
CNTL Minimum Duty-Cycle Threshold		0.20		0.26	V
CNTL Maximum Duty-Cycle Threshold		1.9		2.1	V
LSYNC Input Low Voltage				0.8	V
LSYNC Input High Voltage		2.2			V
LSYNC Input Frequency Range		120		280	Hz
LSYNC Minimum Duty Cycle		10			%
SEL Input Low Voltage				0.8	V
SEL Input High Voltage		2.2			V
$\overline{SHDN}$ Input Low Voltage				0.8	V
$\overline{SHDN}$ Input High Voltage		2.2			V
TFLT Charging Current	V_{VFB} > 2.4V or V_{IFB} < 720mV; V_{OLF} < 1.1V; V_{TFLT} = 2.0V	0.60		0.90	μA
	V_{VFB} < 2.05V and V_{IFB} > 880mV; V_{OLF} < 1.1V; V_{TFLT} = 2.0V	-1.0		-0.5	
	V_{VFB} < 200mV or V_{OLF} > 1.3V; V_{TFLT} = 2.0V	2.24		3.36	
TFLT Sink Current	V_{TFLT} = 2.0V	80		190	mA
TFLT Trip Threshold	TFLT rising	2.90		3.10	V
FLT Sink Current	V_{TFLT} = 3.1V; V_{FLT} = 0.4V	1			mA

Note 1: -40°C specifications are guaranteed by design, not production tested.

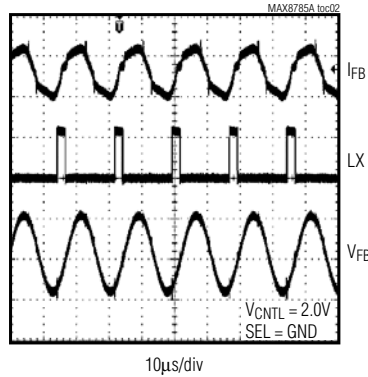# Full-Bridge Controller for Piezoelectric Transformers

(Circuit of Figure 1. V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

LOW INPUT-VOLTAGE OPERATION
(V_{IN} = 12V)

MAX8785A toc01
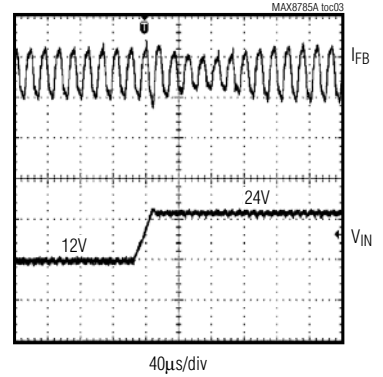
I_{FB}
LX
V_{FB}

V_{CNTL} = 2.0V
SEL = GND

10µs/div
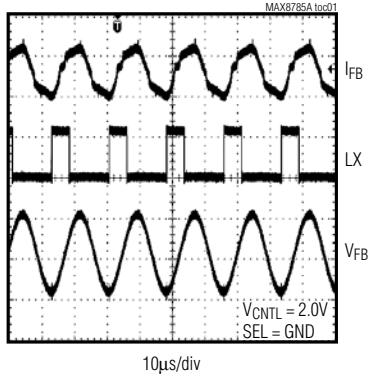
CH1: 10V/div
CH2: 2V/div
CH3: 1V/div

HIGH INPUT-VOLTAGE OPERATION
(V_{IN} = 24V)

MAX8785A toc02

I_{FB}
LX
V_{FB}

V_{CNTL} = 2.0V
SEL = GND

10µs/div

CH1: 20V/div
CH2: 2V/div
CH3: 1V/div

LINE-TRANSIENT RESPONSE

MAX8785A toc03

I_{FB}
24V
12V
V_{IN}

40µs/div

CH2: 2V/div
CH4: 10V/div

MINIMUM BRIGHTNESS OPERATION
AND STARTUP WAVEFORM

MAX8785A toc04

SHDN
COMP
I_{FB}
V_{FB}

4ms/div
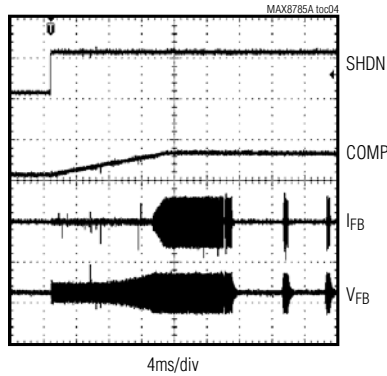
CH1: 2V/div   CH3: 5V/div
CH2: 5V/div   CH4: 2V/div

LSYNC OPERATION

MAX8785A toc05

LSYNC
I_{FB}
LX

1ms/div
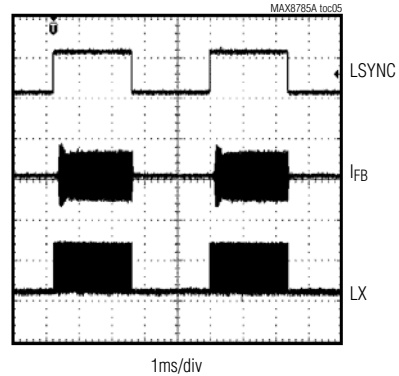
CH1: 2V/div
CH3: 5V/div
CH4: 10V/div

LAMP-OUT VOLTAGE LIMITING
AND TIMEOUT

MAX8785A toc06

V_{FB}
TFLT

200ms/div
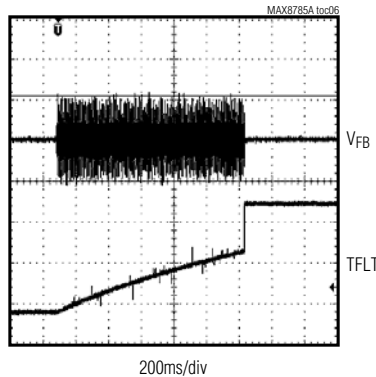
CH1: 2V/div
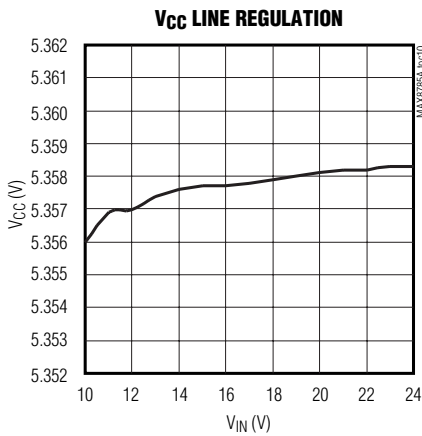CH2: 2V/div

SECONDARY SHORT-CIRCUIT
PROTECTION AND TIMEOUT
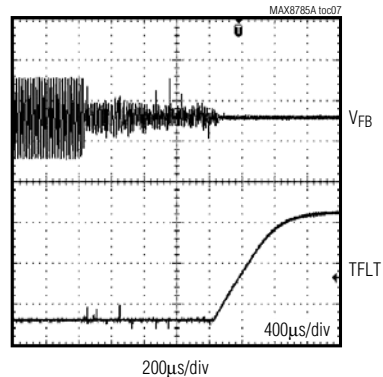
MAX8785A toc07

V_{FB}
TFLT
400µs/div

200µs/div

CH1: 2V/div
CH2: 1V/div

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MAX8785A

Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

MAXIMUM SWITCHING FREQUENCY vs. R_{HF}

MAXIMUM SWITCHING FREQUENCY (kHz) vs. R_{HF} (kΩ)

MAX8785A toc08

DPWM FREQUENCY vs. R_{LF}

DPWM FREQUENCY (Hz) vs. R_{LF} (kΩ)

MAX8785A toc09

V_{CC} LINE REGULATION

V_{CC} (V) vs. V_{IN} (V)

MAX8785A toc10

V_{CC} LOAD REGULATION

V_{CC} REGULATION (%) vs. I_{LOAD} (mA)

MAX8785A toc11

V_{CC} vs. TEMP

V_{CC} (V) vs. TEMPERATURE (°C)

MAX8785A toc12

SWITCHING FREQUENCY vs. V_{IN}

f_{SW} (kHz) vs. V_{IN} (V)

MAX8785A toc13

Full-Bridge Controller for Piezoelectric Transformers

MAX8785A

PIN	NAME	FUNCTION
1	RATE	Duty Ratio Ramp Adjustment Input. Connect a feed-forward network between BATT and RATE to adjust the slope of the internal ramp that adjusts the H-bridge duty cycle with input voltage.
2	$\overline{SHDN}$	Shutdown Control Input. The IC shuts down when $\overline{SHDN}$ is pulled to GND.
3	CNTL	Brightness Control Input. The usable brightness control range is from 0 to 2V. V_{CNTL} = 0 represents the minimum brightness (10% DPWM duty cycle), V_{CNTL} = 2V represents the full brightness (100% DPWM duty cycle). For details, see the *Dimming Control s*ection.
4	LSYNC	DPWM Sync Input. DPWM frequency can be synchronized with an external signal on LSYNC. When SEL is connected to V_{CC}, the duty cycle of the LSYNC signal determines the brightness. For details, see the *Dimming Control* section.
5	FLT	Fault Status Output. FLT is an open-drain output and requires a pullup resistor between V_{CC} and FLT. Under normal conditions, the FLT output is high impedance. FLT pulls low when a fault condition occurs; FLT is reset on either power or $\overline{SHDN}$ cycle.
6	TFLT	Fault Time-Out Setting. Connect a capacitor from TFLT to GND to set the time out period. For details, see the *Setting the Fault Delay Time* section.
7	HF	Maximum Switching Frequency Adjustment Input. Connect a resistor from HF to GND to set the maximum sweeping frequency of the main oscillator.
8	LF	DPWM Frequency Adjustment Input. Connect a resistor from LF to GND to set the DPWM oscillator
9	PCOMP	Phase-Lock Loop (PLL) Compensation Pin. Connect a capacitor between PCOMP and GND to compensate the PLL.
10	COMP	Transconductance Error-Amplifier Output. The COMP voltage controls the voltage-controlled oscillator to adjust the switching frequency. Connect a capacitor from COMP to GND.
11	IFB	Lamp Current-Feedback Input. IFB regulates the average lamp-current feedback to 800mV (typ) by controlling the switching frequency. For details, see the *Lamp-Current Regulation* section.
12	VFB	Secondary Voltage-Feedback Input. A resistive voltage-divider between the high-voltage terminal of the transformer and GND sets the maximum peak lamp voltage during striking and lamp-out fault. Add 1nF capacitor from VFB to GND for noise rejection. For details, see the *Lamp-Out Detection and Overvoltage Protection* section.
13	LX2	GH2 Gate-Driver Return. LX2 is the input to the primary current-limit comparator. The controller senses the voltage across the low-side MOSFET (LX2 - PGND) for primary overcurrent condition.
14	GH2	High-Side MOSFET Gate-Driver Output
15	BST2	GH2 Gate-Driver Supply Input. Connect a 0.1µF capacitor from LX2 to BST2.
16	V_{DD2}	GL2 Low-Side Gate-Driver Supply Input. Connect V_{DD2} to V_{CC}. Bypass V_{DD2} with a 1µF capacitor to PGND.
17	GL2	Low-Side MOSFET Gate-Driver Output
18	PGND	Power Ground. PGND is the return of GL1 and GL2 gate drivers.
19	GL1	Low-Side MOSFET Gate-Driver Output
20	V_{DD1}	GL1 Low-Side Gate-Driver Supply Input. Connect V_{DD1} to V_{CC}. Bypass V_{DD1} with a 1µF capacitor to PGND.
21	BST1	GH1 Gate-Driver Supply Input. Connect a 0.1µF capacitor from LX1 to BST1.
22	GH1	High-Side MOSFET Gate-Driver Output
23	LX1	GH1 Gate-Driver Return. LX1 is the input to the primary current-limit comparator. The controller senses the voltage across the low-side MOSFET (LX1 - PGND) for primary overcurrent condition.

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PIN	NAME	FUNCTION
24	OLF	Arc Fault-Detection Input. When the peak voltage on OLF rises above the internal threshold of 1.2V (typ), an internal current source starts charging the TFLT capacitor. The MAX8785A sets the fault latch and disables the gate drivers after the TFLT voltage reaches 3V. For details, see *Setting the Arc Protection Threshold* section.
25	SEL	Brightness Control Select Input. Brightness can be adjusted with an analog voltage on CNTL or with an external signal at LSYNC. Connect SEL to GND to enable analog control. Connect SEL to V_{CC} to enable external synchronization control.
26	V_{CC}	5.35V/20mA Linear-Regulator Output. Supply voltage for the device. Bypass V_{CC} with a 1µF ceramic capacitor to GND.
27	GND	System Ground
28	BATT	Supply Input. Input to the internal 5.35V linear regulator that powers the device. Bypass BATT to ground with a 0.22µF ceramic capacitor.
29	PAD	Backside Exposed Pad. PAD is internally connected to GND. Connect the exposed pad to a ground plane through a thermally enhanced via.

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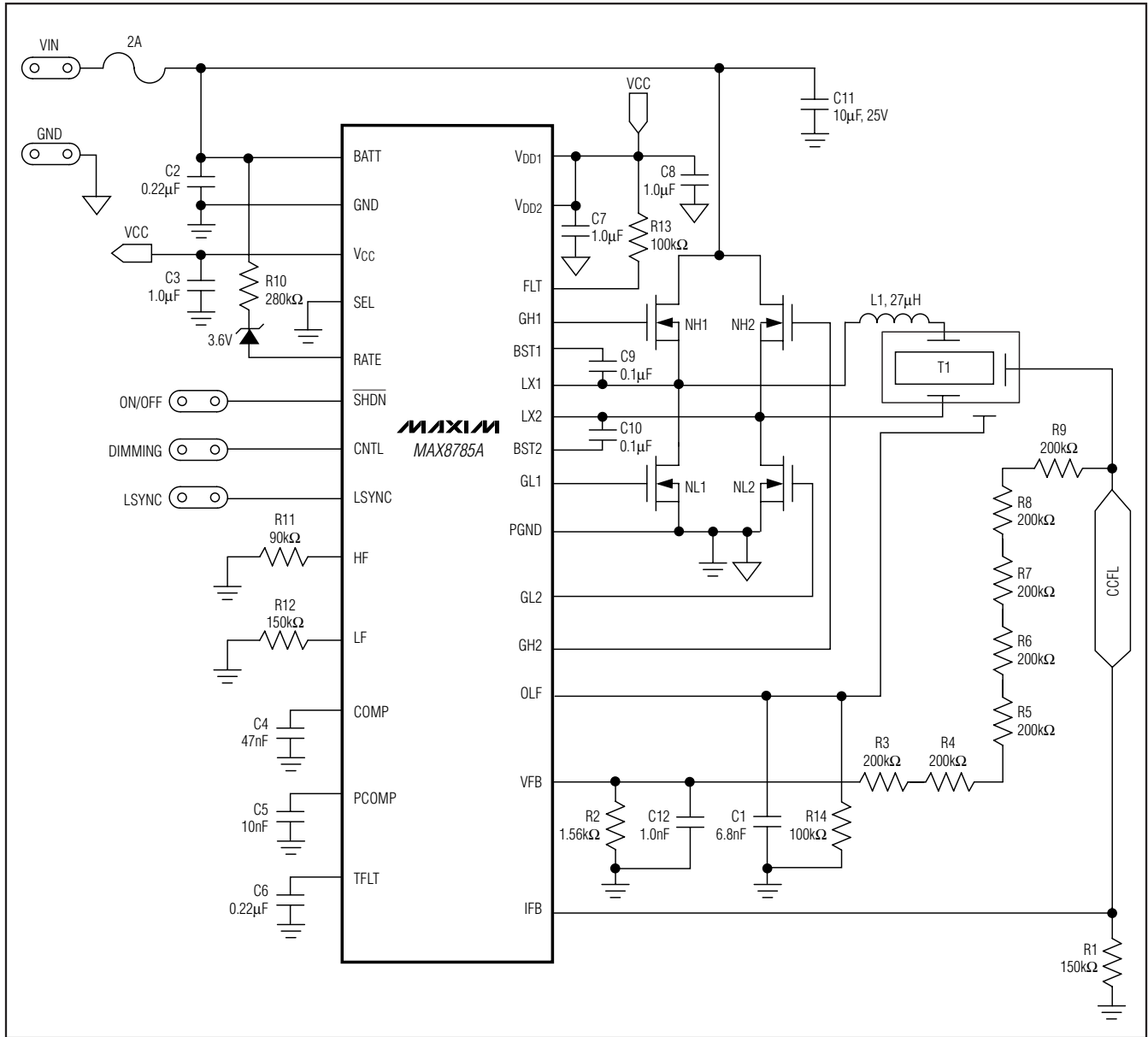# Full-Bridge Controller for Piezoelectric Transformers

MAX8785A

Figure 1. Typical Operating Circuit
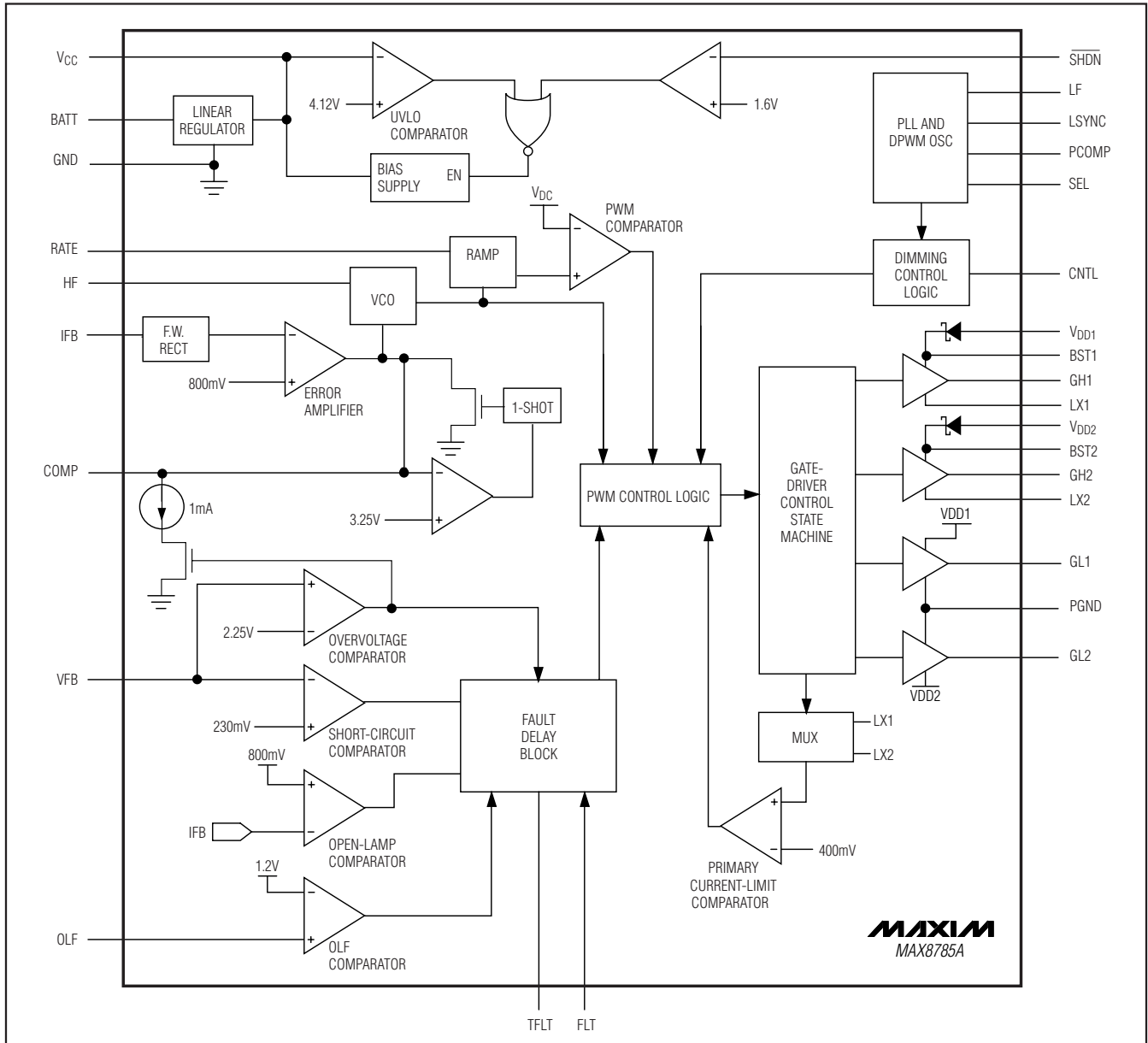
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Block Diagram

Figure 2. MAX8785A Block Diagram

Detailed Description

The MAX8785A is a full-bridge CCFL controller for piezo-electric transformer-based CCFL inverters. The full-bridge topology provides a high-spectral purity sinusoidal drive to help efficiently operate the piezoelectric transformer. The MAX8785A uses feed-forward control to adjust the duty cycle that effectively regulates lamp current during line transients and maintains relatively constant switching frequency. The rate of the feed-forward ramp signal can be adjusted with an external resistor to accommodate different input voltage ranges and different types of piezoelectric transformers.
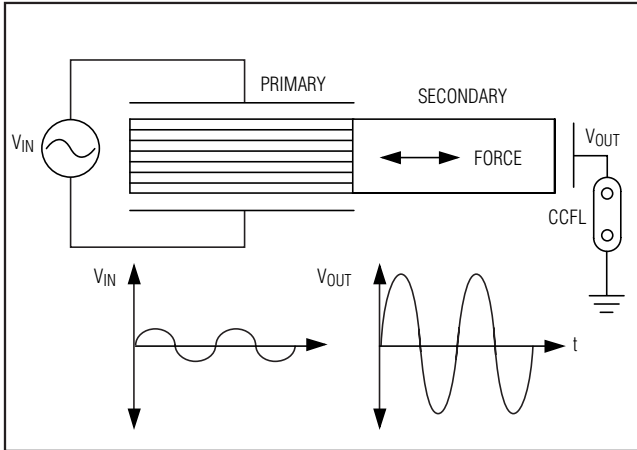
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Figure 3. Typical Multilayer PZT in Longitudinal Mode

Figure 4. Electrical Model of Piezoelectric Transformer

Figure 5. Voltage Ratio vs. Frequency for Resonant Tank

The MAX8785A can achieve 10:1 dimming range with the DPWM method. CCFL brightness can be adjusted using analog or digital dimming control. Analog voltage on CNTL controls duty ratio of DPWM and an external resistor on LF (R_{LF}) controls the frequency of DPWM. The digital signal on LSYNC controls the duty ratio and frequency of DPWM.

The MAX8785A guarantees lamp striking by sweeping the switching frequency from high to low until the lamp strikes. The maximum switching frequency can be adjusted with an external resistor. The MAX8785A voltage-controlled oscillator changes the switching frequency to regulate the lamp current.

The MAX8785A provides protection against lamp arc, open lamp, secondary short circuit, and primary overcurrent. The MAX8785A includes an adjustable fault delay timer and an open-drain fault indicator. The MAX8785A has primary current limiting by using lossless current sensing to prevent overstressing the power MOSFETs.

Piezoelectric Transformer (PZT) Background

Piezoelectric transformers transfer energy from primary to secondary through use of mechanical force. Figure 3 shows that when electric potential is applied to the primary of the piezoelectric material, the electrical energy is converted into mechanical vibrations (reverse piezoelectric effect). These mechanical vibrations are coupled into the secondary piezoelectric material, and then the piezoelectric material converts the mechanical vibrations to electrical energy (direct piezoelectric effect).

A piezoelectric transformer has a voltage gain from primary to secondary. The voltage gain of the transformer changes with the excitation frequency of the primary. A simplified electrical model that predicts the gain of a
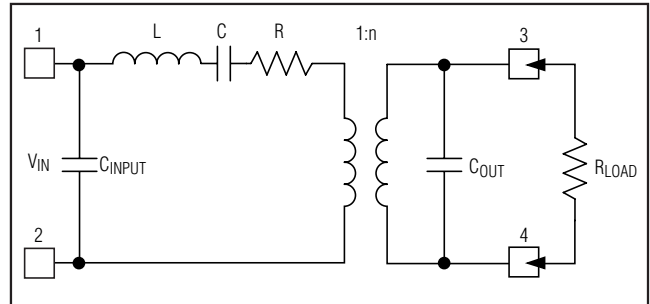
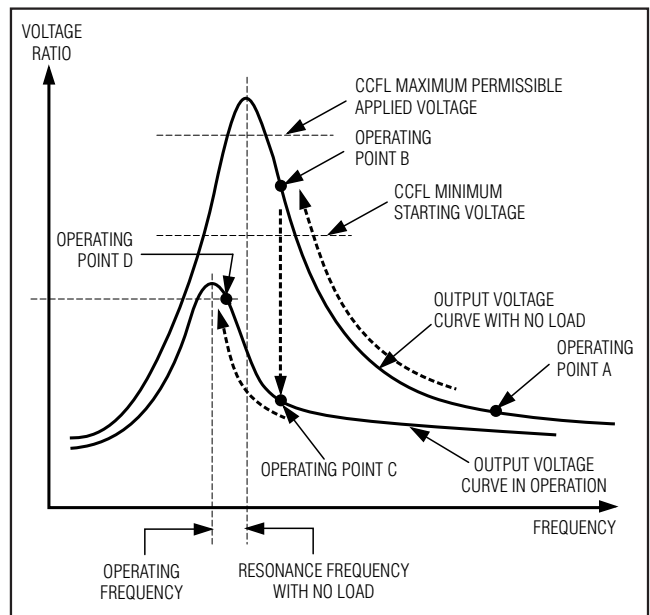piezoelectric transformer is shown in Figure 4. Terminals 1 and 2 are the primary and terminals 3 and 4 are the secondary of the transformer. Many PZT manufacturers provide component values for the model based on measurements taken at various frequencies and output loads.

Figure 5 shows the variation of voltage gain with frequency. During startup, the lamp is not ionized, and therefore, has a no-load condition, so the piezoelectric transformer operates on a high-gain, high-impedance load line. Since the exact strike voltage and operating frequency are not known, the MAX8785A applies a relatively low voltage to the lamp by operating at the maximum-programmed operational frequency. This is shown as Point A. As the operating frequency is decreased, the piezoelectric transformer gain moves up the no-load curve until the CCFL strike voltage is reached. This is shown as operating Point B. At Point B,

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the CCFL strike voltage is reached and the lamp impedance begins to decrease. The operating frequency continues to decrease as the lamp impedance drops until the correct operating point is reached, somewhere between Points C and D. Figure 5 shows the Q of resonant tank is very high. If the operating frequency is close to resonant frequency, then the high Q gives a very high efficiency for the converter. However, due to the high Q, the frequency of operation has to be very close to the resonant frequency, and this reduces the range of the switching frequency for the inverter. To ensure optimal performance, careful selection of external components is required.

Variable Frequency Operation

The MAX8785A includes a voltage-controlled oscillator (VCO) that sets the switching frequency of the H-bridge. The VCO is controlled by the output of a transconductance error amplifier that integrates the difference between the full-wave, rectified lamp-current feedback signal (IFB) and an internal reference voltage (800mV typ). As the lamp current-feedback signal changes with respect to the reference, the error amplifier sources and sinks current, which appropriately adjusts COMP, and equivalently, the VCO frequency.

To strike the CCFL, a frequency sweep is initiated by linearly ramping the COMP capacitor. As the COMP voltage rises, the VCO sweeps the switching frequency from the maximum value (set by the R_{HF} resistor) to the point where the gain of resonant tank is enough to strike the lamp. The frequency sweep range is 15% of the maximum switching frequency.

Feed-Forward Control

The MAX8785A has feed-forward control, which maintains tight control of the lamp current over the entire input voltage range. The feed-forward control adjusts the on-time (t_{ON}) by varying the slope of internal ramp. The current into RATE determines the slope of the internal ramp. Connect a passive network between V_{IN} and RATE to change the duty ratio with input voltage. The RATE pin allows the user to adjust the maximum duty ratio (D_{MAX}) to achieve the optimum performance of the PZT used in the application.

Connect a resistor between BATT and RATE to set D_{MAX}:

$$R_{RATE} = D_{MAX}(\%) \times R_{HF}(k\Omega) \times V_{MIN}(V)$$

where R_{HF} is the resistor that sets the maximum switching frequency and V_{MIN} is the minimum input voltage of operation. The feed-forward network required is dependent upon the PZT used in the application. Further improvements in the performance at higher input voltages can be achieved by adding a zener diode in series with the RATE resistor. The MAX8785A has built-in protection to limit the maximum duty cycle to 45%.

Dimming Control

The MAX8785A has both analog and digital inputs to control brightness.

Analog Dimming Control

Connect SEL to GND to enable analog control mode. The voltage at CNTL controls DPWM duty cycle. The DPWM frequency is externally set by the resistor at LF (R_{LF}). In analog control mode, the adjustment range is 10% to 100%. CNTL has a voltage range of 0 to 2V with 256 brightness levels. Figure 6 shows the response of DPWM duty cycle to the CNTL voltage. When V_{CNTL} is between 0V and 0.23V, the DPWM duty cycle is fixed at 10%. When V_{CNTL} is 0.23V to 2V, the DPWM duty cycle changes linearly with CNTL. When the CNTL voltage is above 2V, the DPWM duty cycle is fixed at 100%.
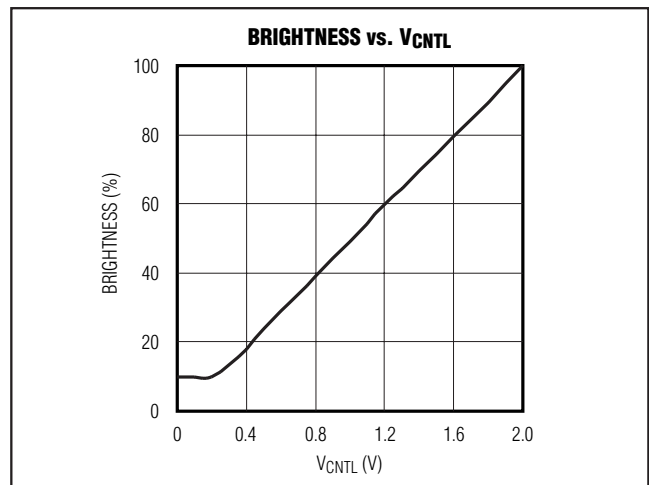

Figure 6. Brightness vs. V_{CNTL}

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The frequency of the internal DPWM oscillator is adjustable through a resistor connected between LF and GND. The DPWM frequency is given by:

$$f_{DPWM} \approx 208Hz \times 150k\Omega / R_{LF}$$

The adjustable range of the DPWM frequency is 100Hz < f_{DPWM} < 300Hz, with a corresponding programming resistance of 103kΩ < R_{LF} < 315kΩ.

External Digital (DPWM) Control

Connect SEL to V_{CC} and an external digital signal at LSYNC to enable digital control mode. DPWM duty ratio and frequency are the same as LSYNC duty ratio and frequency. The frequency range of the digital signal is 120Hz to 280Hz. The range of duty ratio for LSYNC is 10% to 100%, and for correct lamp operation, the duty cycle should always be above 10%. When the duty ratio of LSYNC is 100%, the CCFL is at full brightness.

A phase-lock loop (PLL) is used to synchronize the internal DPWM signal with the externally applied digital signal at LSYNC. PLL is a feedback system that operates on the excess phase of a periodic signal. Connect a capacitor from PCOMP to GND to stabilize the PLL. To ensure fast response of the PLL, connect a 10nF capacitor from PCOMP to GND.

Lamp-Current Regulation

The MAX8785A uses a lamp-current control loop to regulate the CCFL current. The control loop is a transconductance amplifier as shown in Figure 2. The AC lamp current is sensed with a sense resistor connected in series with the low-voltage terminal of the lamp. The IFB input is internally full-wave rectified. The transconductance error amplifier compares the average value of the rectified IFB voltage with 800mV (typ) internal reference. The output of the transconductance error amplifier V_{COMP} controls a VCO, which sets the switching frequency of the inverter.

Lamp Startup

A CCFL is a gas-discharged lamp that is normally driven in the avalanche mode. To start ionization in a non-ionized lamp, the applied voltage (striking voltage) must be increased to the level required to start the flow of current. For example, the normal running voltage of a typical CCFL is approximately 650V_{RMS}, but the striking voltage can be as high as 1800V_{RMS}.

The MAX8785A's control architecture ensures striking of the lamp. As the COMP voltage rises, the VCO sweeps the switching frequency from the switching frequency (set by the R_{HF} resistor) to the point where the gain of resonant tank is sufficient to strike the lamp. At startup,

the MAX8785A overrides the external DPWM setting and forces 100% brightness setting until the lamp strikes and the lamp current reaches regulation. After the current reaches regulation, the MAX8785A switches to normal DPWM operation using the brightness control mode defined by the SEL pin.

Secondary Short-Circuit Protection

The MAX8785A provides protection against short circuit at the high-voltage terminal of the PZT or excessive leakage from a high-voltage terminal to ground. The MAX8785A senses secondary voltage through the VFB pin (see Figure 1). If the sensed voltage stays below the 230mV threshold for more than the fault time set by the TFLT cap, the MAX8785A disables the gate drivers to avoid excessive output current. The fault time is determined by charging the TFLT capacitor with a 2.8mA current to 3V. When the TFLT fault latch is set, the MAX8785A stops switching and FLT is pulled low.

UVLO

The MAX8785A includes a V_{CC} undervoltage-lockout (UVLO) feature. If V_{CC} is below 4.12V (typ), the high-side and low-side switch gate drivers are disabled and the fault latch is set.

Low-Power Shutdown

When $V_{\overline{SHDN}}$ < 0.8V, all functions of the IC are turned off except the V_{CC}. In shutdown, the linear-regulator output voltage is 4.6V (typ) and the supply current is 10µA (typ). While in shutdown, the arc protection, lamp-out detection, and short-circuit detection latches are reset.

Lamp-Out Detection and Overvoltage Protection

The IFB pin monitors the lamp current to detect faulty or open CCFL lamps. If the peak IFB voltage is less than 800mV, a fault is detected and the MAX8785A charges the TFLT capacitor with a 0.75µA current source. If the voltage on TFLT exceeds 3V, the fault latch is set.

During the lamp-out detection period, the MAX8785A decreases the switching frequency in an effort to strike the lamp. This can result in very high secondary voltage. To address this problem, the MAX8785A includes an overvoltage-protection circuit. The lamp voltage is sensed at the VFB pin, and once the secondary voltage exceeds the overvoltage threshold of 2.25V (typ), an internal 1.0mA current source discharges the COMP node. When COMP discharges, the inverter's switching frequency increases, thereby reducing the gain of the resonant tank and limiting the secondary voltage.

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Open PZT Protection

The MAX8785A has protection against faulty connections of PZT to the PC board. The OLF pin is used to detect high-voltage conditions on the secondary side of the transformer. When the OLF voltage exceeds 1.2V (typ), a 2.8mA current source starts charging the TFLT capacitor. When V_{TFLT} exceeds the threshold of 3V, the fault latch is set and the MAX8785A stops switching. For details, see the *Setting the Arc Protection Threshold* section.

Primary Side Current Limit

The MAX8785A senses the voltage across both low-side MOSFETs at LX1 and LX2. If the voltage exceeds the internal 400mV (typ) current-limit threshold, the MAX8785A turns off the respective MOSFET to prevent the transformer primary current from increasing further.

Applications Information

MOSFETs

The MAX8785A requires four external n-channel power MOSFETs to form a full-bridge inverter circuit to drive the transformer primary. When selecting the MOSFET, focus on the voltage rating, current rating, on-resistance ($R_{DS(ON)}$), total gate charge, and power dissipation.

Select a MOSFET with a voltage rating at least 25% higher than the maximum input voltage of the inverter. For example, if the maximum input voltage is 24V, the voltage rating of the MOSFET should be 30V or higher. The current rating of the MOSFET should be higher than the peak primary current at the minimum input voltage and full brightness. Use the following equation to estimate the primary peak current I_{PEAK_PRI}:

$$I_{PEAK\_PRI} = \frac{\sqrt{2} \times P_{OUT\_MAX}}{V_{IN\_MIN} \times \eta}$$

where P_{OUT_MAX} is the maximum output power, V_{IN_MIN} is the minimum input voltage, and η the estimated efficiency at the minimum input voltage, assuming the full bridge drives one CCFL and maximum output power of 4.5W. If the minimum input voltage is 8V and the estimated efficiency is 75% at that input, the peak primary current is approximately 1.1A. Therefore, power MOSFETs with a DC current rating of 1.4A or greater are sufficient.

Since the regulator senses the on-state, drain-to-source voltage of both MOSFETs to detect the transformer primary current, the lower the MOSFET $R_{DS(ON)}$, the higher the current limit would be. Therefore, the user should select n-channel MOSFETs with low $R_{DS(ON)}$ to

minimize conduction loss, and keep the primary current limit at a reasonable level. Use the following equation to estimate the maximum and minimum values of the primary current limit:

$$I_{LIM\_MIN} = \frac{370mV}{R_{DS(ON)\_MAX}}$$

$$I_{LIM\_MAX} = \frac{430mV}{R_{DS(ON)\_MIN}}$$

Both MOSFETs must be able to dissipate the conduction losses, as well as the switching losses at both V_{IN_MIN} and V_{IN_MAX}. Calculate both terms. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of the MOSFETs. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider choosing MOSFETs with lower parasitic capacitance. If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the conduction losses equal the switching losses.

Calculate the total conduction power dissipation of the two MOSFETs using the following equation:

$$PD_{CONDUCT} = I_{PRI}^2 \times R_{DS(ON)}$$

where I_{PRI} is the primary current calculated using the following equation and $R_{DS(ON)}$ is MOSFET on-resistance:

$$I_{PRI} = \frac{P_{OUT\_MAX}}{\eta \times V_{IN}}$$

where P_{OUT_MAX} is the output power of the lamp.

Both MOSFETs turn on with the ZVS condition, as the switching frequency is the same as the resonance frequency of the tank, so there is no switching power dissipation associated with high-side MOSFET. However, the current is at peak when the MOSFET is turned off. Calculate the total turn-off switching power dissipation of the two MOSFETs using the following equation:

$$PD_{SWTICH} = \frac{\sqrt{2} \times C_{RSS} \times V_{IN}^2 \times f_{SW} \times I_{PRI}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of the MOSFETs, and I_{GATE} is the peak gate-drive sink current when the MOSFET is being turned off.

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Setting the Lamp Current

The MAX8785A senses the lamp current flowing through resistor R1 (Figure 1) connected between the low-voltage terminal of the lamp and ground. The voltage across R1 is fed to IFB and is internally full-wave rectified. The MAX8785A controls the desired lamp current by regulating the average of the rectified IFB voltage. To set the RMS lamp current, select R1 as follows:

$$R1 = \frac{\pi \times 800mV}{2\sqrt{2} \times I_{LAMP(RMS)}}$$

where $I_{LAMP(RMS)}$ is the desired RMS lamp current, and 800mV is the typical value of the IFB regulation point. To set the RMS lamp current to 6mA, the value of R1 should be 148Ω. The closest standard 1% resistors are 147Ω and 150Ω. The precise shape of the lamp-current waveform depends on lamp parasitics. The resulting waveform is an imperfect sinusoid waveform, which has an RMS value that is not easy to predict. A high-frequency true RMS current meter (such as Yokogawa 2016) should be used to measure the RMS current and make final adjustments to R1. Insert this meter between the sense resistor and the lamp's low-voltage terminal to measure the actual RMS current.

Setting the Secondary Voltage Limit

The MAX8785A limits the transformer secondary voltage during lamp-out conditions. The secondary voltage is sensed through a resistive voltage-divider, as shown in Figure 1. The voltage at VFB is proportional to the CCFL voltage. The total resistance from the HV side to ground should be greater than 1MΩ so that the resistive voltage-divider does not affect normal lamp operation. Resistors R2 and R3 through R9 set the maximum secondary voltage limit. The resistance of R2 can be calculated as follows :

$$R2 = \frac{V_{FB\_OV} \times R_{VFB}}{V_{LAMP\_MAX}}$$

where R_{VFB} = R3 + R4 + R5 + R6 + R7 + R8 + R9 = 1.4MΩ and VFB_OV is the overvoltage threshold. To set the maximum lamp voltage to 2000V with R_{VFB} = 1.4MΩ, R2 must be equal to 1.54kΩ. The voltage across each resistor during normal operation should not exceed its voltage rating; hence, the number of resistors in R_{VFB} can be calculated from the following equation:

$$n = \frac{LampOperatingVoltage \times 1.4}{V_{SEC\_MAX}}$$

Assuming the normal lamp operating voltage is 800V and the resistor voltage rating is 200V, then n = 5.6. Choose six resistors for the VFB string.

Setting the Arc Protection Threshold

If during normal operation, the PZT loses contact with the PC board, the MAX8785A stops switching. This feature is referred to as arc protection. During normal operation when the PZT-to-PC board connection is broken, a very high voltage develops between the terminals, resulting in arcing. The arcing is detected using a capacitive voltage-divider from the PZT high-voltage side to the OLF pin. Figure 7 shows an equivalent high-voltage capacitor between the bottom layer of the PZT and the metal layer of the PC board. The lower layer of the PZT and metal layer of the PC board creates a high-voltage capacitor. Terminals 1 and 2 are the primary side of the PZT, terminal 3 is the secondary side, and terminal 4 is the metal layer of the PC board, which is the low-voltage side of the capacitor (C_{PZT}).
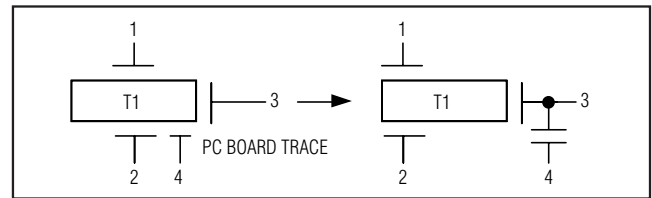

Figure 7. Arc Protection

C_{PZT} and C1 in Figure 1 form a capacitive voltage-divider to OLF pin. These capacitors set the maximum secondary voltage for an ARC fault. C1 can be calculated from the following equation:

$$C1 = \frac{\sqrt{2} \times V_{LAMP(RMS)\_MAX}}{1.2V} \times C_{PZT}$$

C_{PZT} should be measured on the board. Refer to the MAX8785A EV Kit data sheet for suggested layout.

COMP Capacitor Selection

COMP is the output of the transconductance error amplifier for the lamp-current control loop. Connect a capacitor between COMP and GND to stabilize the current-control loop. The value of COMP capacitance determines the response time of the lamp-current control loop. The COMP capacitance also determines the power-on startup timing. The recommended COMP capacitance is 47nF.

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Setting the Fault Delay Time

The TFLT capacitor determines the delay time for both open-lamp fault and arc fault. The MAX8785A charges the TFLT capacitor with a 0.75µA current source during open-lamp fault and charges the TFLT capacitor with a 2.8mA current source during an arc fault and secondary short circuit. The MAX8785A sets the fault latch when the TFLT voltage reaches 3V. Use the following equations to calculate the open-lamp fault delay (t_{OPEN_LAMP}), arc fault (t_{ARC}), and secondary short-circuit delay ($t_{SHORT\_CIRCUIT}$):

$$t_{OPEN\_LAMP} = \frac{C_{TFLT} \times 3V}{0.75\mu A}$$

$$t_{ARC} = \frac{C_{TFLT} \times 3V}{2.8mA}$$

$$t_{SHORT\_CIRCUIT} = \frac{C_{TFLT} \times 3V}{2.8mA}$$

Bootstrap Capacitors

The high-side gate drivers are powered using two bootstrap circuits. The MAX8785A integrates the bootstrap diodes so only two 0.1µF bootstrap capacitors are needed. Connect the capacitors between LX1 and BST1 and between LX2 and BST2 to complete the bootstrap circuits.

Layout Guidelines

Careful PC board layout is important to achieve stable operation. The high-voltage sections and the switching section of the circuit require particular attention. The high-voltage sections of the layout need to be well separated from the control circuit. Follow these guidelines for good PC board layout:

1) Keep the high-current paths short and wide, especially at the ground terminals. This is essential for stable, jitter-free operation and high efficiency.

2) Use a star ground configuration for power and analog grounds. The power and analog grounds should be completely isolated, meeting only at the center of the star. The center should be placed at the analog ground pin (GND).

3) Route high-speed switching nodes away from sensitive analog areas (V_{CC}, RATE, HF, LF, COMP, and TFLT).

4) Mount the decoupling capacitor from V_{CC} to GND as close as possible to the IC with dedicated traces that are not shared with other signal paths.

5) The current-sense paths for LX to GND must be made using Kelvin-sense connections to guarantee the current-limit accuracy. With 8-pin SO MOSFETs, this is best done by routing power to the MOSFETs from outside using the top copper layer, while connecting GND and LX inside (underneath) the 8-pin SO package.

6) Ensure the feedback connections are short and direct. To the extent possible, IFB, VFB, and OLF connections should be far away from the high-voltage traces and the transformer.

7) To the extent possible, high-voltage trace clearance on the transformer's secondary should be widely separated. The high-voltage traces should also be separated from adjacent ground planes to prevent lossy capacitive coupling.

Full-Bridge Controller for Piezoelectric Transformers

Simplified Operating Circuit
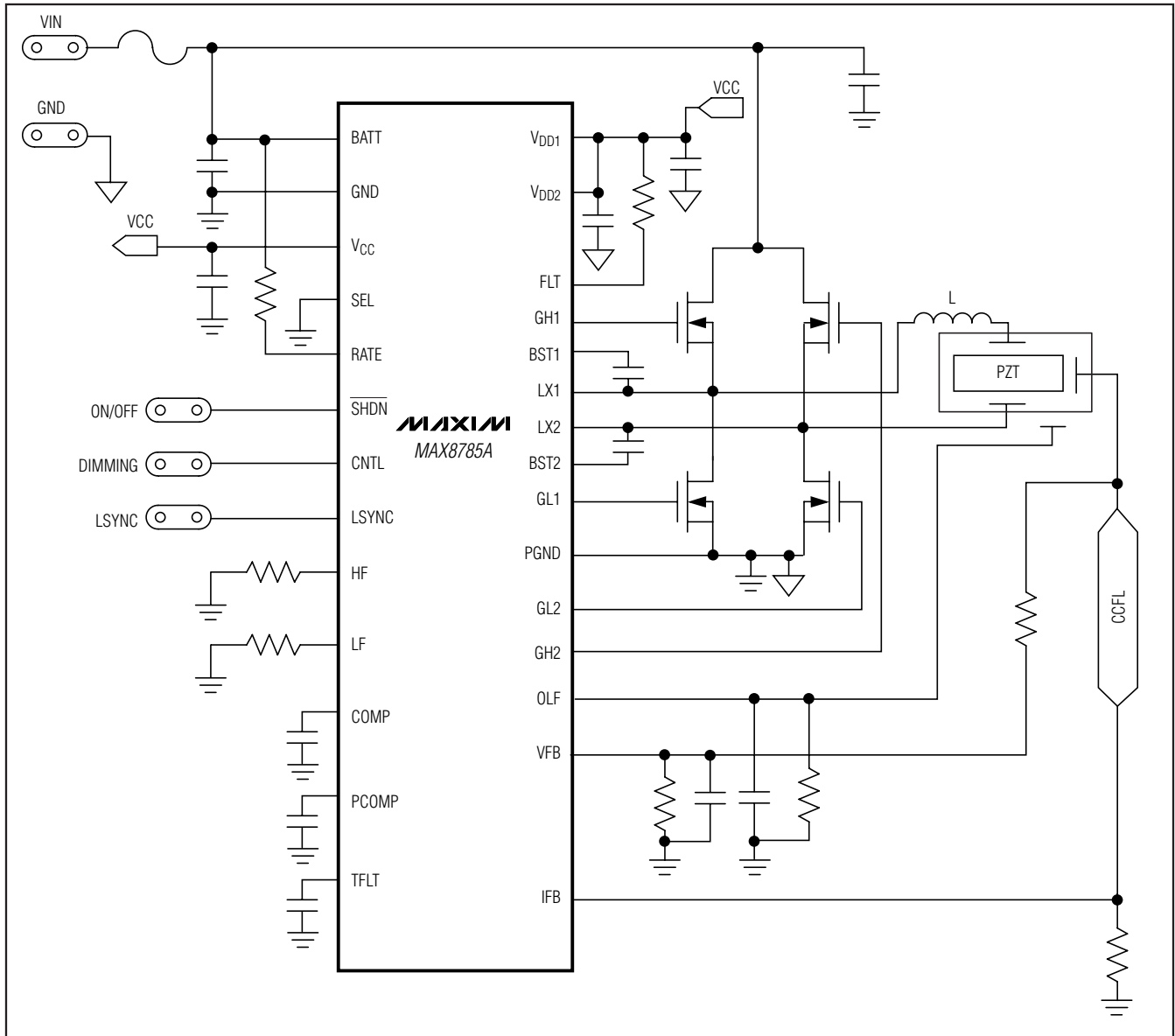
Chip Information

TRANSISTOR COUNT: 6281

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TQFN	T2855-6	**21-0140**

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Full-Bridge Controller for Piezoelectric Transformers

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/06	Initial release	—
1	6/08	Replacing MAX8785 with A version	1–19

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