PIC18F2220/2320/4220/4320

PIC18F2220/2320/4220/4320 Rev. C1 Silicon Errata

The PIC18F2220/2320/4220/4320 Rev. C1 parts you have received conform functionally to the Device Data Sheet (DS39599**G**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2220/2320/4220/4320 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F2220/2320/4220/4320 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2220	0000 0101 100	0 0110
PIC18F2320	0000 0101 000	0 0110
PIC18F4220	0000 0101 101	0 0110
PIC18F4320	0000 0101 001	0 0110

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F2220/2320/4220/4320 silicon.

1. Module: Core (DAW Instruction)

The DAW instruction may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the DAW instruction. If the Carry bit is set, increment the next higher byte to be added, using an instruction such as INCFSZ (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the DAW instruction has been executed, process the Carry bit normally (see Example 1).

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```
MOVLW   0x80       ; .80 (BCD)
ADDLW   0x80       ; .80 (BCD)

BTFSC   STATUS, C  ; test C
INCFSZ  byte2      ; inc next higher LSB
DAW
BTFSC   STATUS, C  ; test C
INCFSZ  byte2      ; inc next higher LSB

This is repeated for each DAW instruction.
```

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: MSSP (All I^2C™ and SPI Modes)

The Buffer Full flag bit (BF) of the SSPSTAT register (SSPSTAT<0>) may be inadvertently cleared, even when the SSPBUF register has not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = `1111`) and
- Any instruction that contains C9h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

Identified work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh.

In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the Access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select all GPR Banks.
2. If accessing a part of Bank 15 is required and the use of Access Banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contain C9h in the 8 Least Significant bits while the BSR points to Bank 15 (BSR = 0Fh).

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: MSSP (SPI, Slave Mode)

In its current implementation, the $\overline{SS}$ (Slave Select) control signal generated by an external master processor may not be successfully recognized by the PIC® microcontroller operating in Slave Select mode (SSPM3:SSPM0 = `0100`). In particular, it has been observed that faster transitions (those with shorter fall times) are more likely to be missed than slower transitions.

Work around

Insert a series resistor between the source of the $\overline{SS}$ signal and the corresponding $\overline{SS}$ input line of the microcontroller. The value of the resistor is dependent on both the application system's characteristics and process variations between microcontrollers. Experimentation and thorough testing is encouraged.

This is a recommended solution; others may exist.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Oscillator

The 32 kHz internal oscillator, INTRC, will be held in Reset if either of the following is enabled:

- Power-up Timer
- High-Speed Crystal/Resonator with PLL Enabled (HSPLL) Oscillator mode

Without the INTRC oscillator running, the Power-up Timer and Phase Locked Loop (PLL) timer will not expire and the PIC18F2220/2320/4220/4320 device will not exit Reset. This issue does not affect the Watchdog Timer or any other mode.

The provided work arounds require only two modifications to the Configuration Word values. No additional changes to the application hardware or software are necessary, except as noted below.

Work around: Power-up Timer

Disable the Power-up Timer by programming $\overline{\text{PWRTEN}}$ (CONFIG2L<0>) to '1'. This results in a shorter time before the microcontroller begins to execute code after power up or exiting from Sleep mode or from Brown-out Reset (if enabled).

If a power-up delay is needed to ensure a stable V_{DD}, consider using the Brown-out Reset (BOR) feature. The BOR keeps the device in Reset until the specified V_{DD} has been achieved.

This work around is available by programming the $\overline{\text{BOR}}$ bit to '1' and selecting BOR voltage bits with BORV<1:0> bits in the CONFIG2L Configuration Word.

If $\overline{\text{BOR}}$ is not enabled and additional start-up delay is needed, consider implementing an external system supervisor to keep the microcontroller in Reset until the V_{DD} has stabilized. Alternately, consider use of an equivalent PIC18F4321 device.

Work around: HSPLL Oscillator Mode

Two work arounds are available through the Configuration bits. Enabling either of the following features permits the HSPLL mode to work successfully:

- Two-Speed Start-up
- Fail-Safe Clock Monitor

Both options permit the microcontroller to start from the 32 kHz INTRC after power-up, BOR, or wake-up from Sleep mode. The options also permit code to execute while PLL is waiting to lock.

The PLL lock time typically is 2 ms which results in approximately 16 instruction executions before the switch to the HSPLL clock occurs. If typical initialization code is performed after a Power-on Reset or Brown-out Reset, the impact of this work around should be negligible.

If Sleep mode is used, both work arounds result in code execution during PLL lock time. A software delay may be needed to avoid executing time-critical code after wake-up. The OSTS (OSCCON<3>) bit will set to indicate when the HSPLL is ready and time-critical code can be executed.

The Two-Speed Start-up and Fail-Safe Clock Monitor work arounds switch the system clock source from INTRC to HSPLL mode after a PLL lock occurs. This is handled automatically by the microcontroller and requires no additional software or special monitoring. For more information, see **Section 2.7 "Clock Sources and Oscillator Switching"** in the *"PIC18F2220/2320/4220/4320 Data Sheet"* (DS39599).

Date Codes that pertain to this issue:

Engineering and production devices with a date code of 0813 or later may be affected.

REVISION HISTORY

Rev A Document (9/2008)
First revision of this document. Includes silicon issues 1 (Core – DAW Instruction), 2 (MSSP – All I^2C™ and SPI modes), 3 (MSSP – SPI, Slave Mode) and 4 (INTRC Oscillator).

Rev B Document (1/2009)
Changed title of silicon issue 4 (Oscillator).

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