Dual 4-bit static shift register BU4015B / BU4015BF

The BU4015B and BU4015BF are 4-stage static shift registers, each consisting of two circuits.

The D flip-flops for each stage share a common reset input, enabling external asynchronous reset at any point.

Also, the flip-flops at each stage are triggered by the rising edge of the clock input.

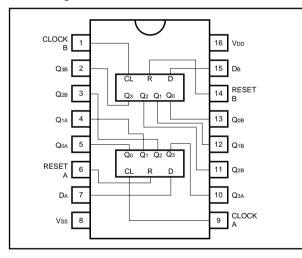
"H" level reset input resets the contents of all stages to "L", regardless of the clock and data input, and sets data outputs Q0 to Q3 to "L".

Features

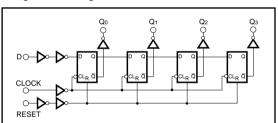
- 1) Low power dissipation.
- 2) Wide range of operating power supply voltages.
- 3) High input impedance.

- 4) High fan-out.
- 5) Direct drive of 2 L-TTL inputs and 1 LS-TTL input.

Block diagram



Logic circuit diagram



Truth table

CLOCK	D	RESET	Q_0	Q ₁	Q_2	Q ₃	
	L	L	L	Q_0	Q ₁	Q_2	
	Н	L	Н	Q ₀	Q ₁	Q ₂	
¬ <u>L</u>	Х	L	No Change				
X	Х	Н	L	L	L	L	

X : Irrelevant

●Absolute maximum ratings (Vss = 0V, Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{DD}	- 0.3 ~ + 18	V
Power dissipation	Pd	1000 (DIP), 500 (SOP)	mW
Operating temperature	Topr	- 40 ~ + 85	°C
Storage temperature	Tstg	- 55 ~ + 150	°C
Input voltage	Vin	- 0.3 ~ V _{DD} + 0.3	V

•Electrical characteristics

DC characteristics (unless otherwise noted, Ta = 25°C, Vss = 0V)

Parameter	Symbol	Min.	Тур.	Max.	Unit	V _{DD} (V)	Conditions
Input high level voltage	Vıн	3.5	_	_		5	
		7.0	_	_	V	10	<u> </u>
		11.0	_	_		15	
Input low level voltage	VIL	_	_	1.5	V	5	
		_	_	3.0		10	_
		_	_	4.0		15	
Input high level current	lін	_	_	0.3	μΑ	15	V _{IH} = 15V
Input low level current	lıL	_	_	- 0.3	μΑ	15	VIL = 0V
Output high level voltage	Vон	4.95	_	_	V	5	lo = 0mA
		9.95	_	_		10	
		14.95	_	_		15	
Output low level voltage	Vol	_	_	0.05	V	5	lo = 0mA
		_	_	0.05		10	
		_	_	0.05		15	
	Іон	- 0.16	_	_	mA	5	Vон = 4.6V
Output high level current		- 0.4	_	_		10	Vон = 9.5V
		- 1.2	_	_		15	Vон = 13.5V
	loL	0.44	_	_	mA	5	Vol = 0.4V
Output low level current		1.1	_	_		10	Vol = 0.5V
		3.0	_	_		15	Vol = 1.5V
	lob	_	_	20	μА	5	
Static current dissipation		_	_	40		10	VI = VDD or GND
		_	_	80		15	

Switching characteristics (unless otherwise noted, Ta = 25°C, Vss = 0V, CL = 50pF)

	Symbol	Min.	Тур.	Max.	Unit		0 111
Parameter						V _{DD} (V)	Conditions
Output rise time	tт∟н	_	180	_	ns	5	
		_	90	_		10	_
		_	65	_		15	
Output fall time	tтн∟	_	100	_	ns	5	
		_	50	_		10	_
		_	40	_		15	
	tplн tpнL	_	310	_		5	
Propagation delay time, CLOCK, D→Q		_	125	_	ns	10	<u> </u>
		_	90	_		15	
Propagation delay time, RESET to Q	tplн tpнL	_	460	_	ns	5	
		_	180	_		10	_
RESET IO Q		_	120	_		15	
	tsu	_	100	_	ns	5	
Setup time		_	50	_		10	<u> </u>
		_	40	_		15	
	twh (CLK)	_	185	_	ns	5	
Minimum clock pulse width		_	85	_		10	_
puise widin		_	55	_		15	
	twh (R)	_	200	_	ns	5	
Minimum reset pulse width		_	80	_		10	<u> </u>
puise width		_	60	_		15	
	f (CLK) Max.	_	20	_	MHz	5	
Maximum clock frequency		_	6.0	_		10	_
		_	7.5	_		15	
	tr (CLK) tr (CLK)	_	100	_	μs	5	
Maximum clock rise time and fall time		_	40	_		10	_
and and tall tille		_	15	_		15	
Input capacitance	Cin	_	5	_	pF	_	_

Measurement circuits

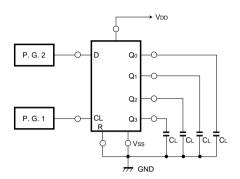


Fig.1 Switching characteristics measurement circuit

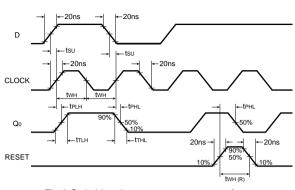
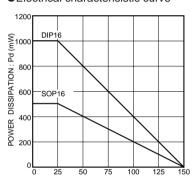


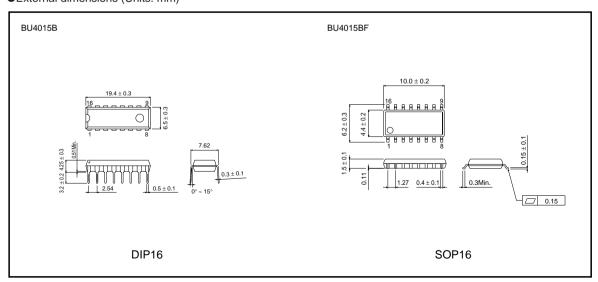
Fig.2 Switching time measurement waveform

•Electrical characterisistic curve



AMBIENT TEMPERATURE: Ta (°C)
Fig.3 Power dissipation vs.
ambient temperature

External dimensions (Units: mm)



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