RFDA0025

DIGITAL CONTROLLED VARIABLE GAIN AMPLIFIER

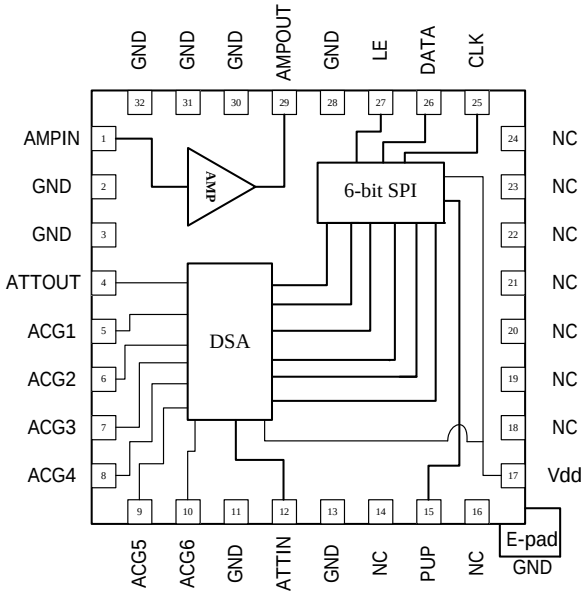
Package: MCM 32-Pin, 5.2mmx5.2mm

Features

- 50MHz to 850MHz Operation
- 6-Bit Digital Step Attenuator
- Serial Control Interface
- 31.5dB Attenuation Range (0.5dB Step)
- High OIP3/P1dB=+42/20dBm
- Single +5V Supply
- Footprint Compatible with 32-Pin 5mmx5mm QFN

Applications

- Transceiver IF DVGA
- Cellular, PCS, 3G Infrastructure
- Wireless Data, Satellite Terminals



Functional Block Diagram

Product Description

RFMD's RFDA0025 is a digital controlled variable gain amplifier featuring high linearity over the entire gain control range. The 6-bit digital step attenuator is programmed with a serial mode control interface. The RFDA0025 is packaged in a small 5.2mmx5.2mm leadless laminate MCM with plated through thermal vias for ultra low thermal resistance. The footprint for this module is directly compatible with most 32-pin 5mmx5mm QFNs. The amplifier's bias choke and DC blocks are external, allowing for optimum performance over specific bands within 50MHz to 850MHz.

Ordering Information

RFDA0025SQ	Sample bag with 25 pieces
RFDA0025SR	7" Reel with 100 pieces
RFDA0025R7	7" Reel with 750 pieces
RFDA0025R13	13" Reel with 2500 pieces
RFDA0025PCK-410	50MHz to 850MHz PCBA with 5-piece sample bag

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☑ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ BiFET HBT
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC}, V_{DD})	5.5	V
Collector Current (I_C)	115	mA
Power Dissipation	630	mW
Input RF Power	+20	dBm
Operating Temperature (T_{CASE})	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Junction Temperature (T_J)	+150	°C
ESD Rating (HBM)	Class 1B	
Moisture Sensitivity Level	MSL 3	

Notes: 1. PDISS=VCC*I_C-RF Output Power+RF Input Power

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Frequency	50		850	MHz	
Gain - 150MHz (Max Gain State)		18.7		dB	Attenuation=0dB, 150MHz
Gain - 850MHz (Max Gain State)	16.2	17.7	19.2	dB	Attenuation=0dB, 850MHz
Gain Control Range		31.5		dB	0.5dB LSB, 6 bits
Step Accuracy	±(0.1 +5% attenuation setting)			dB	Major state max error
Output IP3 - 150MHz		42		dBm	150MHz, P_{OUT}=0dBm/tone, 1MHz spacing
Output IP3 - 850MHz	33	35		dBm	850MHz, P_{OUT}=0dBm/tone, 1MHz spacing
Output P1dB	17	20		dBm	Attenuation=0dB
Input Return Loss		20		dB	150MHz
Output Return Loss		25		dB	150MHz
Noise Figure		4.7		dB	150MHz, Attenuation=0dB
t_{RISE}, t_{FALL}		250		ns	10/90% RF
Amplifier Supply Voltage (V_{CC})	4.75	5	5.25	V	
Attenuator Supply Voltage (V_{DD})	3.3	5	5.25	V	
Total Supply Current	80	90	100	mA	Sum of currents from V_{DD} and V_{CC}
Thermal Resistance		57		°C/W	
Control Interface	6-Bit, Serial				
Control Voltages	Low, V_{CTL}=0 to 0.8 V_{DC} High, V_{CTL}=2.0 to V_{DD} V_{DC}				

Notes:
1. All measurements based on the 50MHz to 850MHz Application Circuit, T=25°C
2. V_{CC}=V_{DD}=+5V, V_{CTL}=0/5V

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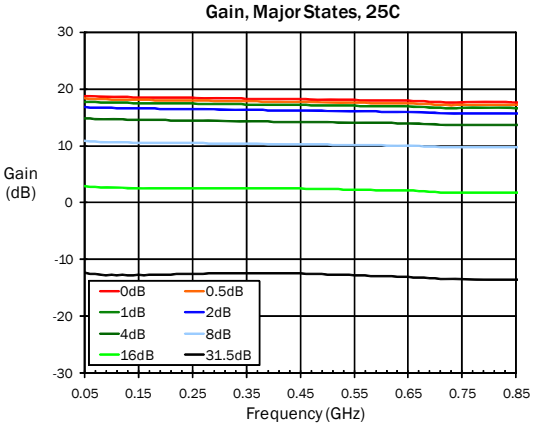
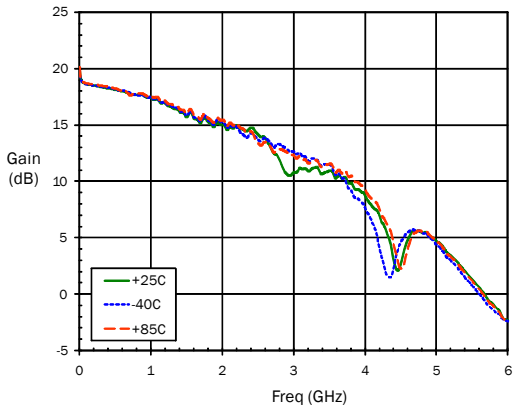
Typical Performance - 50MHz to 850MHz Broadband Application Circuit

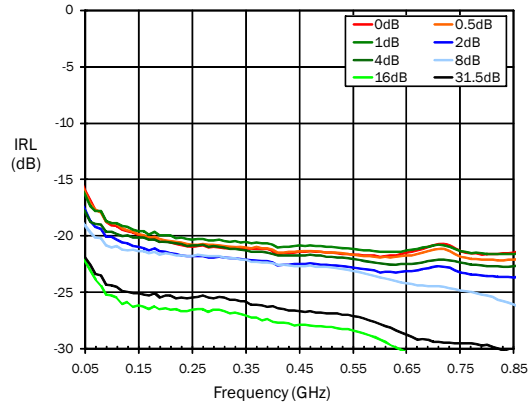
Gain, Major States, 25C



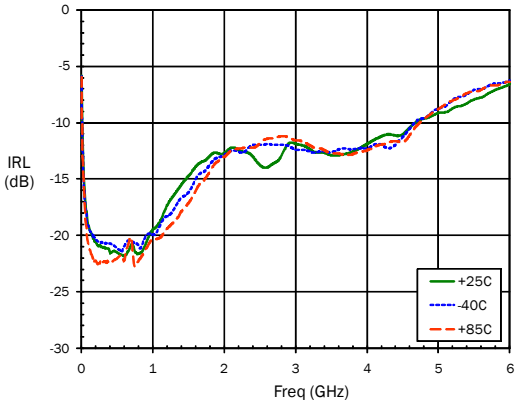
Gain over Temperature, Max Gain



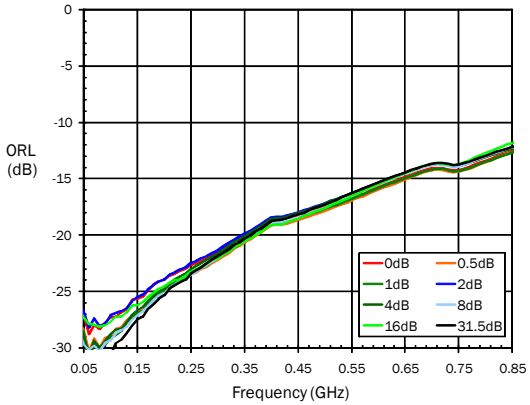
Input RL, Major States, 25C



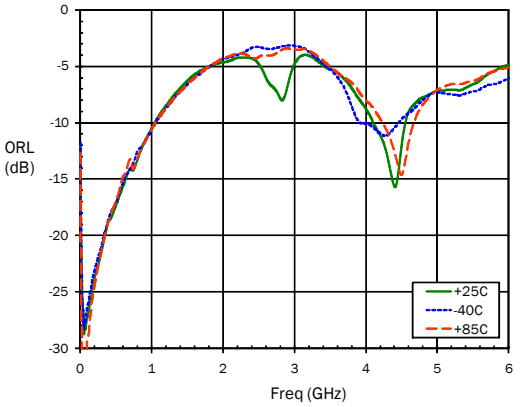
Input RL over Temperature, Max Gain



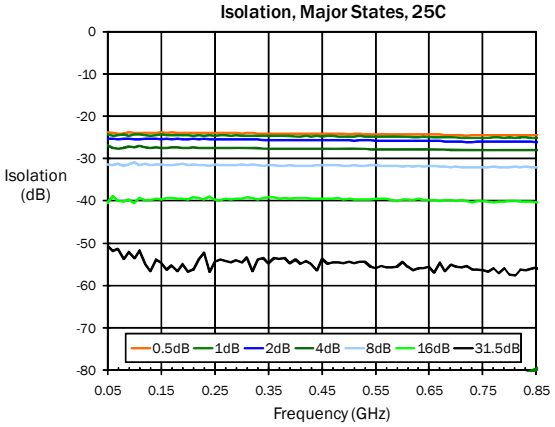
Output RL, Major States, 25C



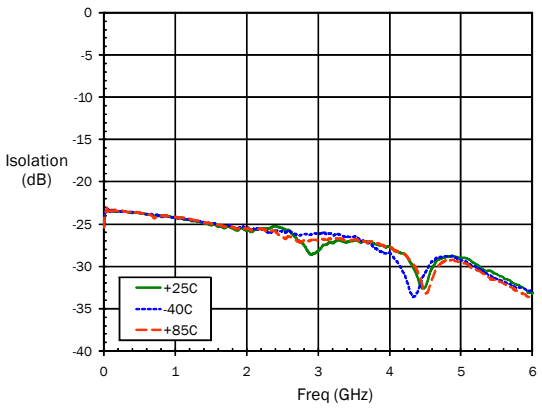
Output RL over Temperature, Max Gain



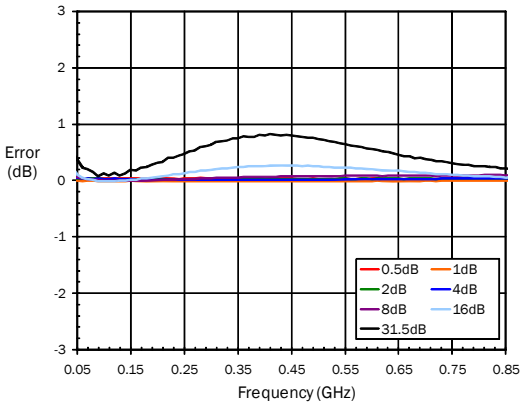
Isolation, Major States, 25C



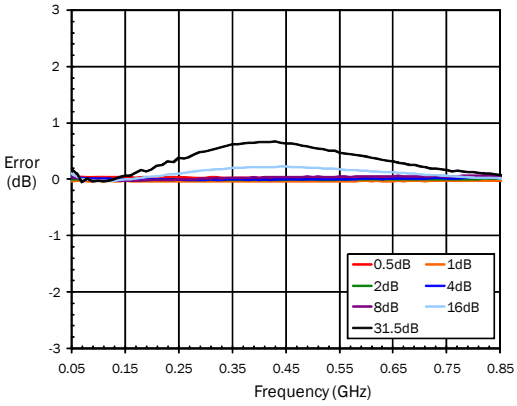
Isolation over Temperature, Max Gain



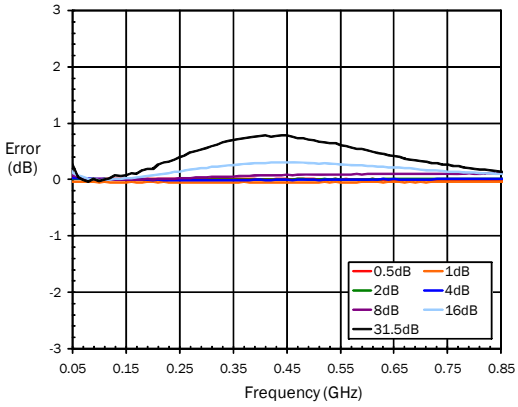
Attenuation Error, Major States, 25C



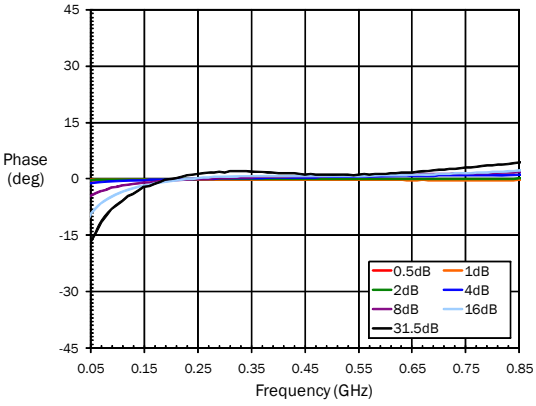
Attenuation Error, Major States, 85C



Attenuation Error, Major States, -40C



Normalized Phase Error, Major States, 25C



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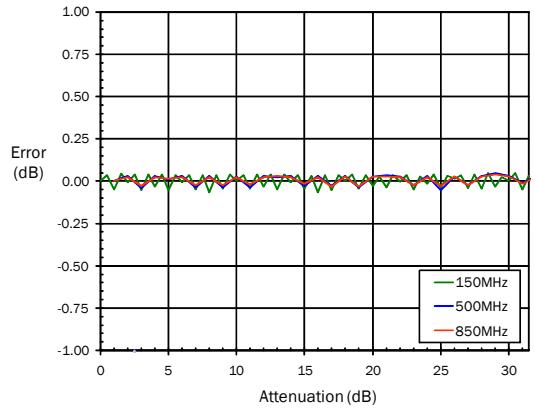
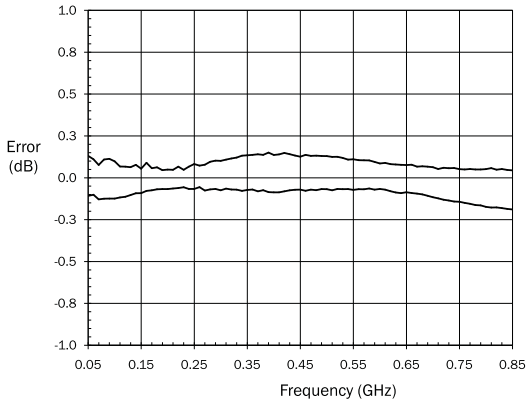
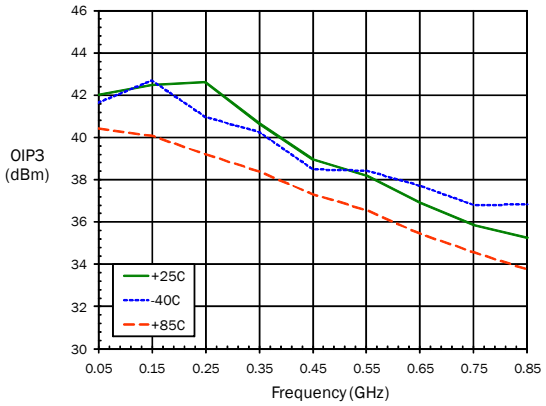
Successive Step Error, 25C



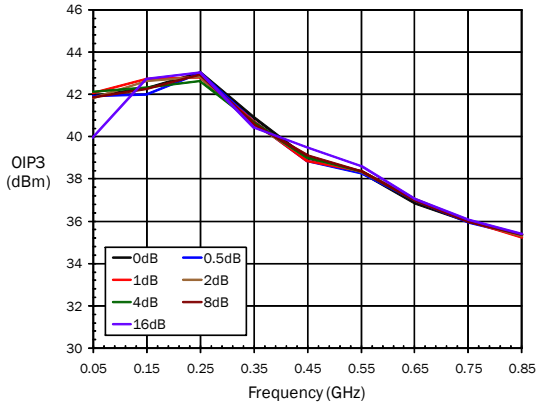
Worst Case Successive Step Error, 25C



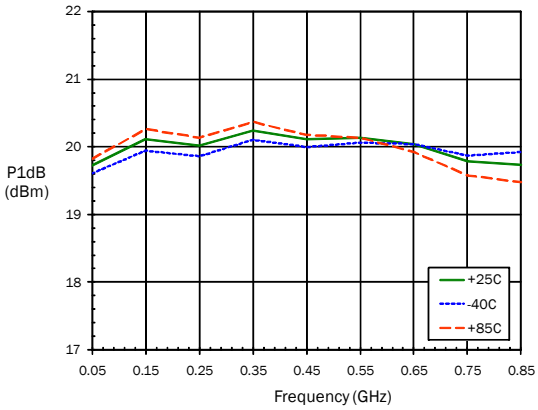
OIP3 over Temperature, Max Gain



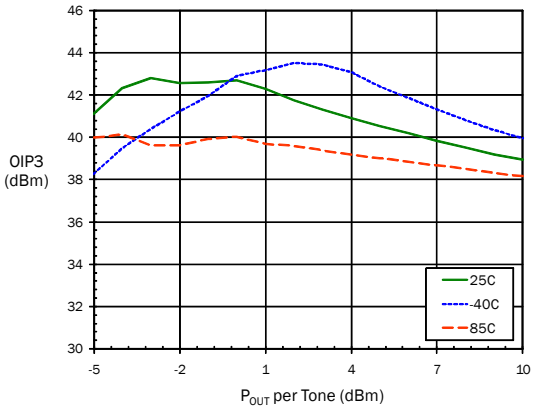
OIP3, Major States, 25C, P_{OUT}/tone=0dBm

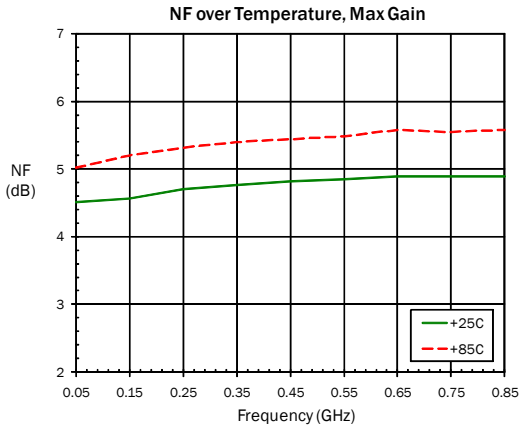


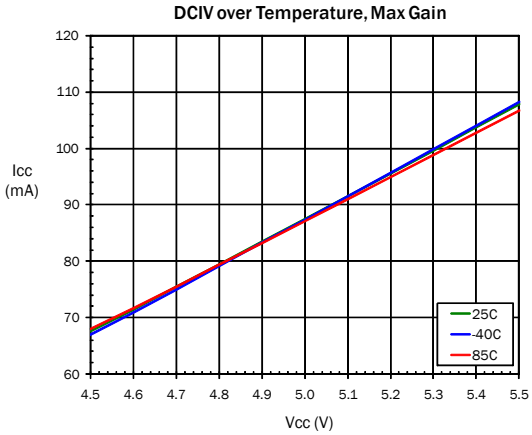
P1dB over Temperature, Max Gain



OIP3 versus P_{OUT}, Max Gain, 150 MHz







Truth Table

DSA Control Bit						Relative Gain Setting
D5 16dB	D4 8dB	D3 4dB	D2 2dB	D1 1dB	D0 0.5dB	
1	1	1	1	1	1	Max Gain
1	1	1	1	1	0	-0.5dB
1	1	1	1	0	1	-1dB
1	1	1	0	1	1	-2dB
1	1	0	1	1	1	-4dB
1	0	1	1	1	1	-8dB
0	1	1	1	1	1	-16dB
0	0	0	0	0	0	-31.5dB

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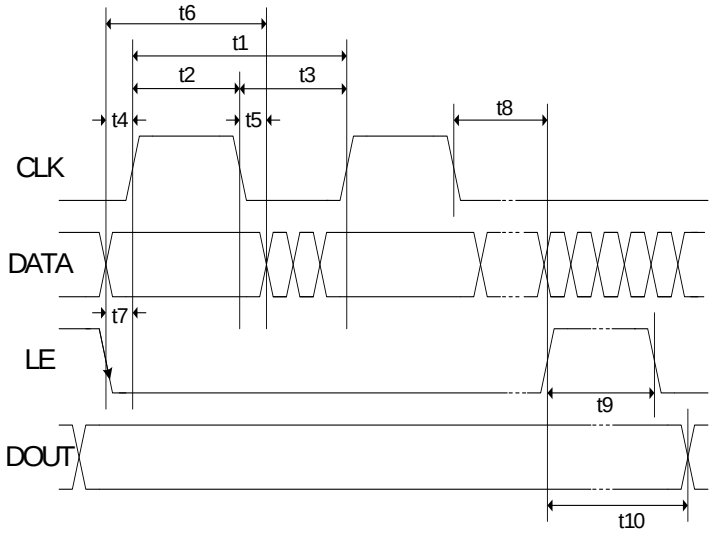
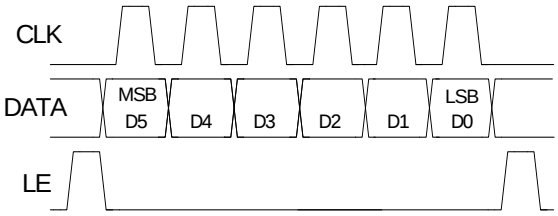
Serial Port Interface:

SPI Timing Diagram



Programming Example - 6-Bit



SPI Timing Diagram Specifications

Parameter	Limit	Unit	Comment
t1	25	MHz max	CLK Frequency
t2	20	ns min	CLK High
t3	20	ns min	CLK Low
t4	5	ns min	DATA to CLK Setup Time
t5	5	ns min	DATA to CLK Hold Time
t6	30	ns min	DATA Valid
t7	5	ns min	LE to CLK Setup Time
t8	5	ns min	CLK to LE Setup Time
t9	10	ns min	LE Pulse Width
t10	20	ns max	Output Set

Control Voltage Table		
State	V_{DD}=+3V	VDD=+5V
Low	0V to 0.8V	0V to 0.8V
High	2.0 to V_{DD}	2.0 to V_{DD}

Power-up Programming Truth Table	
PUP	Attenuator Setting
Low	Attenuation at Max, 31.5dB
High	Attenuation at Min, 0dB

Pin Names and Description

Pin	Function	Description
1	AMPIN	Amplifier Input. DC Block Required.
2	GND	RF/DC Ground Connection.
3	GND	RF/DC Ground Connection.
4	ATTOUT	Digital Attenuator Output. DC Block Required.
5	ACG1	External bypass capacitor required for F < 500MHz (impacts step error).
6	ACG2	External bypass capacitor required for F < 500MHz (impacts step error).
7	ACG3	External bypass capacitor required for F < 500MHz (impacts step error).
8	ACG4	External bypass capacitor required for F < 500MHz (impacts step error).
9	ACG5	External bypass capacitor required for F < 500MHz (impacts step error).
10	ACG6	External bypass capacitor required for F < 500MHz (impacts step error).
11	GND	RF/DC Ground Connection.
12	ATTIN	Digital Attenuator Input. DC Block Required.
13	GND	RF/DC Ground Connection.
14	NC	No Internal Connection.
15	PUP	Power-up Programming Pin. Low=Max Attenuation at Power-up (-31.5dB). High=Min Attenuation at Power-up (0dB).
16	NC	No Internal Connection.
17	VDD	Digital Attenuator Supply Voltage.
18	NC	No Internal Connection.
19	NC	No Internal Connection.
20	NC	No Internal Connection.
21	NC	No Internal Connection.
22	NC	No Internal Connection.
23	NC	No Internal Connection.
24	NC	No Internal Connection.
25	CLK	Serial Clock.
26	DATA	Serial Data.
27	LE	Latch Enable.
28	GND	RF/DC Ground Connection.
29	AMPOUT/VCC	Amplifier Output and Bias. External Choke, Bypassing, and DC Blocks Required.
30	GND	RF/DC Ground Connection.
31	GND	RF/DC Ground Connection.
32	GND	RF/DC Ground Connection.

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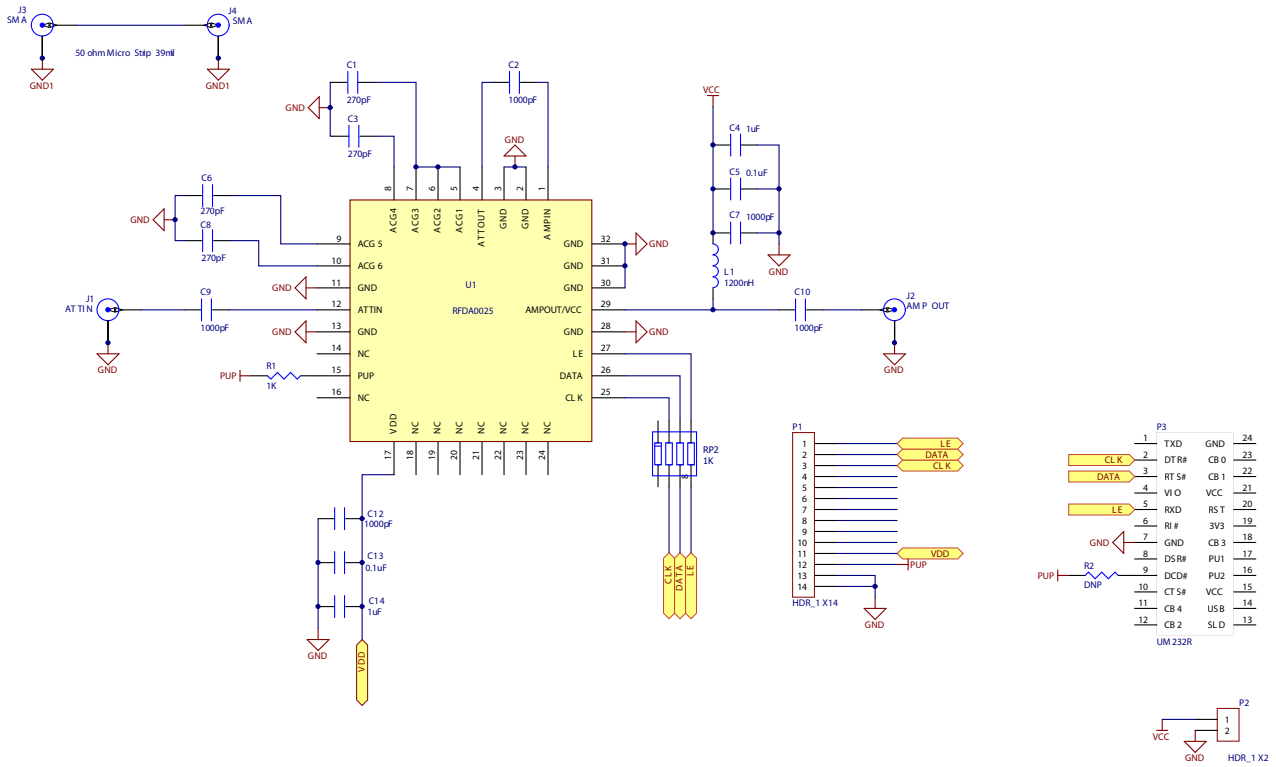
Evaluation Board Schematic

50MHz to 850MHz Application Circuit



Evaluation Board Bill of Materials (BOM)

50MHz to 850MHz Application Circuit

Description	Reference Designator	Manufacturer	Manufacturer's P/N
RDA1005L w/ USB Evaluation Board	PCB Itself	Dynamic Details (DDI) Torronto	RDA1005L410(C)
RFDA0025, 5.2 x 5.2sq. mm,32-Pin Laminate	U1	RFMD	RFDA0025
CAP, 270pF, 5%, 50V, C0G, 0402	C1, C3, C6, C8	Murata Electronics	GRM1555C1H271JA01E
CAP, 1000pF, 10%, 50V, X7R, 0402	C2, C7, C9-C10, C12	Murata Electronics	GRM155R71H102KA01E
CAP, 1µF, 10%, 16V, X7R, 0805	C4, C14	Murata Electronics	GRM21BR71C105KA01K
CAP, 0.1µF, 10%, 16V, X7R, 0603	C5, C13	Murata Electronics	GRM188R71C104KA01D
IND, 1200nH, 5%, W/W, 1008	L1	Coilcraft	1008CS-122XJLC
RES, 1K, 5%, 1/16W, 0402	R1	Kamaya, Inc	RMC1/16S-102JTH
RES ARRAY, 4-ELEM, 1K, 5%, SMD 4 x 0402	RP2	KOA	CN1E4KTTD102J
CONN, HDR, ST, PLRZD, 14-Pin, 0.100"	P1	ITW Pancon	MPSS100-14-C
CONN, HDR, ST, PLRZD, 2-Pin, 0.100"	P2	ITW Pancon	MPSS100-2-C
CONN, SKT, 24-PIN DIP, 0.600", T/H	P3	Aries Electronics Inc.	24-6518-10
CONN, SMA, END LNCH, FLT, 0.062"	J1-J4	Emerson Network Power	142-0701-821
MOD, USB TO SERIAL UART, SSOP-28	M1 (See Note)	Future Technology Devices Int'l	UM232R
DNP	C11, R2, RP3-RP4	N/A	N/A

Note: M1 is to be mounted into P3 with respect to the Pin 1 alignment of M1 and P3

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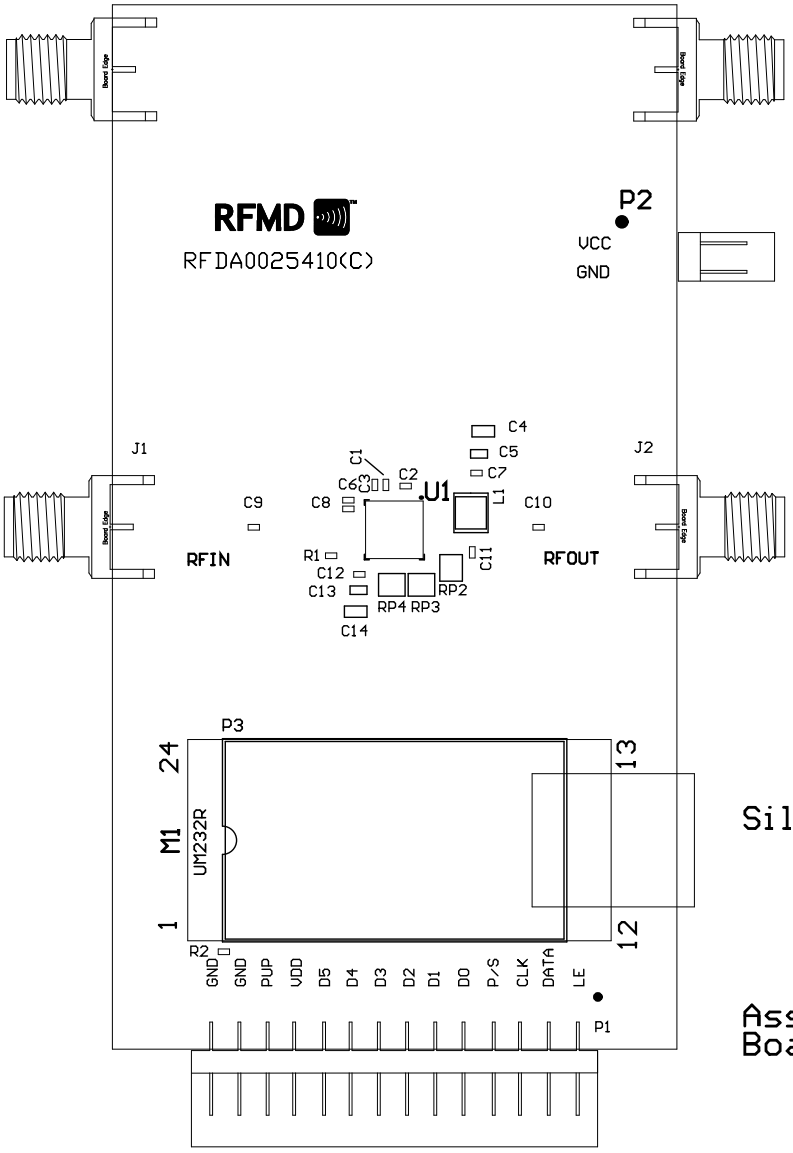
Evaluation Board Assembly Drawing



Silkscreen Top

Assembly Top
Board Outline

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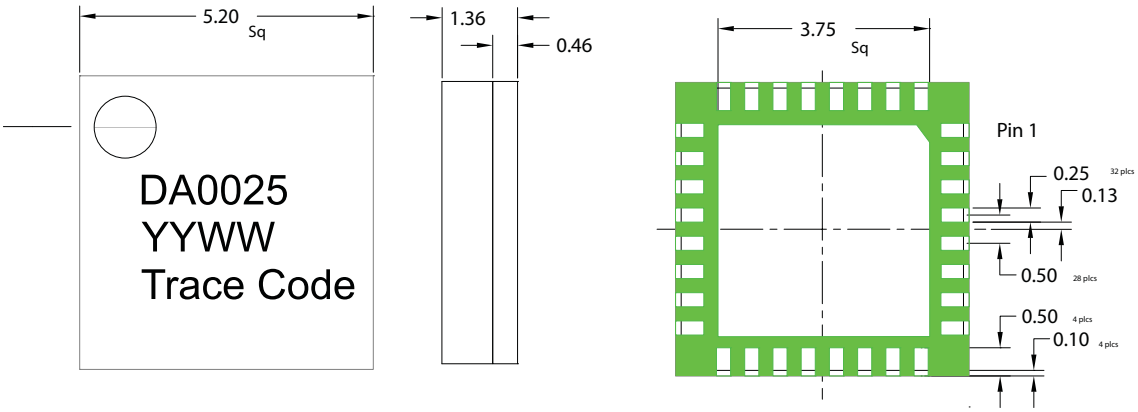
Package Drawing

5.2mmx5.2mm Laminate Module



Pin 1 Indicator

Dimensions in millimeters

YY = Year
WW = Week

Trace Code to be assigned by SubCon

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